Testing Mixed Signal SOCs

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There are certainly dozens of issues that will make the testing of mixed signal systems-on-a-chip (SOCs) difficult and costly. Many of these issues are the same ones that have been with the testing community for years. But there are a few testing issues that are either unique to mixed signal SOCs or at least are extremely exaggerated in these highly integrated designs. The problems fall into three basic categories: test development time, performance, and production cost.

In the digital realm, the test development problem has been largely overcome by a number of techniques, including ATPG, BIST, etc. These issues are not particularly unique to SOCs. Test development time for the analog and mixed signal portions of mixed signal SOCs has not grown exponentially as it did in the pre-automation days of digital circuits. We haven’t seen the explosive growth in numbers of mixed signal circuits on a single die for a basic reason: there are only so many real-world signals we need to interface with in even a complex SOC device. Our mixed signal test development challenge relates more to the need to merge mixed signal test intellectual property (IP) from multiple sources. Any experienced mixed signal test engineer is familiar with the difficulty of merging mixed signal test code from multiple engineers. Unlike digital patterns which can be spliced together easily, mixed signal code blocks are interrelated due to sampling rate interdependencies, etc. The root cause of this difficulty in merging IP is due to the operating systems and architectures of mixed signal testers. The merged IP problem will be exaggerated in mixed signal SOCs.

The next issue is analog and mixed signal performance. This issue is truly frightening to the experienced mixed signal test engineer who knows how subtle the interactions can be between mixed signal circuits and supposedly independent digital blocks. The only way to avoid these unwanted crosstalk problems is to develop far better simulation and modeling tools so the problems can be identified in the design process. This will require fast, accurate simulations of top level models orders of magnitude beyond the simulations we can run today. Test simulation will also benefit from this needed advance in simulation technology, aiding in the test development time issue.

The third problem area unique to SOCs is the exorbitant cost of single insertion testing of highly integrated devices. We expect a single tester to efficiently generate DC signals, a 1kHz sine wave, an algorithmic flash memory pattern, and a sub-nanosecond timing megavector pattern for digital logic. It would be far more efficient to use a DC tester to perform DC tests if it weren’t for the DUT and data handling issues inherent to multiple insertion testing. It is perhaps time to re-evaluated our demands on one-size-fits-all testers and at least ask the question: Why can’t handlers and ATE testers work in a production line environment, in which each testing process is handled by a machine ideally suited to that task?