TEST: WHEN IS ENOUGH ENOUGH?

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1. Introduction

The focus of this panel is the trade-off between excessive testing and acceptable shipped quality levels. How much testing is enough? We all strive to ship our customers high quality product, or at least product that meets our customers’ quality expectations. Often improvements in shipped quality levels can be made by plugging obvious holes in a device’s test suite, sometimes simply by increasing the fault coverage of an existing test. However, at other times, there are no obvious deficiencies in the test methodology and the hunt begins for new failure mechanisms, fault models, and test methods to detect them. Many times the enhanced tests not only improve the shipped quality level, but also drive an unacceptable decrease in yield. This decrease in yield is the result of catching defects that would have appeared in the field (the intent of enhancing the manufacturing test), but also can be the result of an over zealous culling of manufactured product which results in scrapping product that would never have failed in the field.

2. Upstream/Downstream

Let’s look at test from a board manufacturer’s point-of-view. With the exception of a few special instances, when developing a board level test, we want to create tests to detect those defects which we can effect during the board assembly and manufacturing process. Examples of these defects are open/shorted pins, missing components, misoriented components, poor solder joints, reliability problems, etc. We generally do not want to test for silicon defects. We make the assumption that we are putting good components on the board and need to test for the defects that we ourselves can cause, not that come from upstream.

Board manufacturers correctly feel that we should not be expected to detect silicon defects at board test, when we have restricted access to the components and the tester technology is board oriented, not component oriented. One exception to this may be the testing for defects which manifest themselves during the interaction of two separate components, each testing good themselves, but failing to “play well together”. These types of failures might be corrected with tighter specifications at the component level or better board level design.

3. New Test Techniques

Many times, a customer request for a new or different test technique causes concern on the manufacturing floor. The request may be the result of the customer receiving unacceptable quality levels, but often results from the customer’s desire to exercise built-in self test circuitry that will be used in system test or in the field. The BIST may not have any additional value for the component manufacturer, so the question becomes, “If a device passes normal manufacturing test, but fails the extra customer requested test (BIST in this case), who’s problem is it?”

In some cases, new techniques may supply additional fault coverage, but poor diagnostic resolution. In manufacturing, the importance of using a test’s diagnostic information to pinpoint the defect in order to effect a defect reducing process change should not be ignored. A test that is an effective defect screen with poor diagnostic resolution does not improve the reduced yield situation.

4. Test Limits

Some tests are relatively black and white, scan tests for example. Others have a widely varying effect on the yield, based on the setting of some measured parameter which separates the “good” devices from the “bad”. The value of resistance during a parametric test is an example of this. The setting of the $I_{DDQ}$ limit is another example. As the effectiveness of $I_{DDQ}$ testing diminishes with continued scaling, the role of $I_{DDQ}$ testing as a yield reducer will receive increasing scrutiny.

In the author’s opinion, there is no hard-and-fast rule to follow in these situations, other than to consult with your customer and decide on an appropriate test strategy for the device. Sometimes it hurts!