Core Testing and the Core of Testing

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Agrawal traces the development of testing over the last four decades. He points out that there is enough theory and practice to construct solutions for problems of core-based testing. He visualizes the design as consisting of digital logic, memory and analog functions, each of which has its own tests. Boundary-scan and analog test bus can be used to realize a testable system on a chip. He attributes the current crisis of testing to an inadequacy in computer engineer education and suggests a remedy. The key lies in identifying the smallest core of test knowledge that is essential for every electronic system design engineer.

About the Speaker

Vishwani Agrawal is a Distinguished Member of Technical Staff at the Bell Labs (R&D arm of Lucent Technologies) in Murray Hill, New Jersey. He is also a visiting professor at Rutgers University. Agrawal holds a Ph.D. degree from the University of Illinois. He published his first paper on test in 1972, in which he combined a random test generator with D-algorithm. He holds 11 U.S. patents on testing. He is the founding editor-in-chief of the Journal of Electronic Testing: Theory and Applications (JETTA), and a former editor-in-chief of IEEE Design & Test of Computers. He is a Fellow of the IEEE. In 1993, he received the Distinguished Alumnus Award from the University of Illinois.