Challenge Of The 90’s: Testing CoreWare™ Based ASICs

Rochit Rajsuman
LSI Logic
1501 McCarthy Blvd.
Milpitas, CA 95035

Testing of CoreWare based ASICs is emerging as the most challenging problem of the 1990’s. The testing challenge is two fold: first, how to test the embedded cores; and second, how to integrate test-set of a core with other blocks into ASIC level test-set. Each of these problems further compounded by the Intellectual Property (IP) protection issue.

For the first problem, how to test a core, there are a number of solutions: (1) through ASIC functional test; (2) direct test application, while accessing core through I/O muxing; (3) test application through boundary scan or a collar register; (4) Built-In Self-Test (BIST); and (5) proprietary solutions. It should be remembered at all times that there is no one size fits all solution. A solution best suited in a particular situation, may become overly restricted and costly in another design.

When cores are tested through ASIC functional test, detailed knowledge of the ASIC is required and hence its use is limited. This method is best suitable for bus-oriented designs and associated issues are fault coverage, fault latency and difficulty in failure analysis.

Direct I/O muxing brings-out core I/Os to the chip I/Os. It is done by multiplexing each input and output pins to a chip level pin so that patterns can be applied directly. This involves increased delay at the I/Os as well as additional routing constraints.

Boundary scan or a simple shift register as a collar to the core is another possible solution to test the core. In this method, the core I/Os are serially connected by a boundary scan chain and are accessible either through a serial chip-level scan or couple of dedicated pins. The limitations of this method are additional delay, increase in the number of serial scan test cycles as well as larger ATE scan memory and area overhead.

Inclusion of Built-In Self-Test is another possible solution. The limitations of this method are area overhead and limited fault coverage of the core’s analog functions. When an ASIC contains multiple copies of a core, each copy requires its own BIST logic and controller and thus, cumulative area overhead become significantly high.

Proprietary solutions have their own advantages/disadvantages. Proprietary solutions are extremely effective to obtain an optimal design when cores of the same ASIC house are used and fabrication also takes place in the foundry of same vendor. Hence, ASIC vendor with their own CoreWare library face much less problems and able to provide robust and cost effective designs.

The second problem, how to integrate test-set of a core into the test-set of ASIC is largely due to IP protection issue. The availability of test set without encryption or some other mechanism of protection opens the door for cloning. If the core test-set is encrypted, the execution become difficult as well as evaluation of test response become very cumbersome. This problem also become minimal when design is done with the cores of same ASIC vendor who fabricates the design.