THE RETURN OF ASYNCHRONOUS LOGIC

S. B. Furber

Department of Computer Science, The University of Manchester, Oxford Road, Manchester M13 9PL, UK.

Introduction

Asynchronous logic is enjoying a resurgence of interest and is poised to resume a role in commercial electronics which it has not played for a few decades, despite its use in some of the earliest computers.

For the last twenty years electronic design has been dominated by the use of clocks to control communication and state transitions. The clock, like the conductor of an orchestra, keeps all parts of the system synchronized. However, while synchronous operation is essential to the correct functioning of an orchestra, it is not central to the operation of an integrated circuits. An integrated circuit is more like a production line where maintaining a smooth flow of partially completed products is important, but achieving this by forcing exact synchrony throughout the production line is unnecessarily rigid.

There is no doubt that the clock offers a simple control model, as a result of which electronic design has been able to keep pace with and exploit rapid advances in technology. So why should we contemplate discarding the basis of the design methodology which has been so successful?

The Rationale for Asynchronous Logic

Many arguments are offered by supporters of asynchronous design styles in favour of abandoning the clock. The most popular emphasize a particular advantage, such as:

• Low power. Clocked circuits waste power by clocking all parts of the chip whether or not they are doing useful work. Power management by gating clocks to some parts of the circuit is at best coarse-grained. Asynchronous circuits are inherently data driven and are active only when doing useful work.

• Performance. Clocked circuits must be margined for worst-case process, operating and data conditions, and therefore typically operate well below their potential. Asynchronous circuits are self-monitoring and can therefore deliver typical rather than worst-case performance.

• Modularity. A clock is a global signal and global signals, like global variables, impede modularity. Asynchronous design supports data encapsulation, clean interfaces and no global signals - they are the object-oriented paradigm of the hardware domain.

• Electro-Magnetic Compatibility (EMC). The clock, by synchronizing activity, maximizes the AC component of the supply current and generates radio interference at harmonics of the clock frequency. Asynchronous design distributes activity over time and frequency, generating less interference and over a broader spectrum.

• Concurrency. Asynchronous design is a more natural way to express concurrency in hardware.

The Evidence for Asynchronous Logic

There is now compelling evidence that asynchronous design is, indeed, feasible on CMOS VLSI, since several complex asynchronous chips have been built and shown to work. But there is still too little evidence to support the claims outlined above. The work at Philips amply demonstrates power savings (at least within a particular application domain) and their elegant Tangram synthesis tools support the concurrency claim. However, much more needs to be done to validate all these claims.

Perhaps more convincing is the increasing industrial interest. Among the established players, Philips and Sun have invested considerable internal resource in asynchronous technology, and recently Intel has shown active interest. Whenever a significant technology change is foreseen, start-up companies form to exploit the inertia of the multi-nationals, and asynchronous logic can now claim at least two such new companies.

Testing Asynchronous Logic

Before asynchronous logic can gain widespread commercial acceptance, production quality assurance techniques must be proven. This is, perhaps, the final hurdle that still faces the asynchronous design community.

Although asynchronous logic presents additional difficulties for production testing, recent advances in the design for test of asynchronous circuits suggest that these problems are not insuperable. Only when manufacturing volumes reach levels comparable to clocked circuits will this finally be demonstrated, but current indications are that we will not have to wait long to see it resolved.