Who was the Shmoo?

“It was a cute little white, squash-shaped cartoon character created by Al Capp in his comic strip “Li’l Abner,” in 1948, see figure 1. Shmoos bred like rabbits and could produce any object at the drop of a hat. Since they loved to please humans, they would willingly pump out milk, eggs, filet mignon, caviar, or anything else if requested. At first glance Shmoos seemed to herald the arrival of Utopia. Unfortunately, a plethora of Shmoos meant that people quit their jobs, stopped paying taxes, and civilisation as we know it began to degenerate quickly - or so Al Capp sought to demonstrate in his mildly didactic way.”

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1 Shmoo Plotting in MOS Testing

The term Shmoo plotting seems to have arisen from the appearance of its image in plots of pass/fail values of PMOS memory ICs for a range of VDD and VSS values. This type of plot was first made in the early 1970s on simple Teletypes connected to minicomputer systems driving the early ATE systems. They probably represented the first type of graphic display created using computers in IC development. Whether Shmoo was actually seen in the plots or somebody was making an unkind comment on the designer; schmo, means twit in Yiddish, has been lost in the mists of time!

This type of analysis arose because early MOS ICs used PMOS technologies, which were cheap, but had unstable MOSFET threshold voltages coupled with poor device mobility by modern standards. Checking the performance of the MOSFET against the bias voltages was very important for this application. Bipolar circuits generally had superior performance and were less sensitive to parameters such as voltage and temperature. So maximising the performance and stability of MOS ICs was essential if they were to compete against the established bipolar technologies. This implied getting the best performance for the IC given the fundamental MOSFET characteristics the process could reliably manufacture.

Modern test engineers have access to vastly improved ATE and displays, but the principle of Shmoo plotting is the same, to identify the basic characteristics of the MOSFET in the performance of an IC. The capabilities of the MOSFET over different voltages and temperature ranges is known from the fundamental equations. If analysis reveals behaviour other than that expected from a MOSFET charging a capacitor, this needs to be characterised for all process conditions to ensure the IC works as specified when delivered in volume to the customer.

2 How does Shmoo plotting fit into modern IC testing?

Modern IC testing has developed many different techniques each with specific targets for improving quality and controlling the process to improve the yield over the life time of the product. Shmoo plotting of digital ICs is part
of the early product characterisation procedures intended to establish that the design is stable within the process and can be manufactured with virtually zero yield loss, except for spot defects. In this sense Shmoo plotting verifies that the IC has been implemented to six-sigma design principles, or better. It also allows the wafer/batch monitoring parameters to be accurately established for the product. For the vast majority ICs for which no performance binning is performed, it avoids testing all of the parts in production for process variations. This is economically essential for high volume production because testing a device for process variations expressly implies functional testing, instead of simple defect oriented testing such as scan testing or IDDQ. Thus, knowledge gained from Shmoo plotting can be used to optimize the process, design, and final test program.

3 How is a modern Shmoo plot created?

Most modern ATE systems will have a basic software capability to create Shmoo plots. Some ATE vendors focus on production test issues and neglect this capability, whereas others provide excellent Shmoo plotting capabilities with data manipulation built-in. The basic hardware for Shmoo plotting exists within any production ATE, the exception is control of the device’s temperature. This is a mechanical capability added to the tester, it is generally a slow process to control, and is difficult to perform at low temperatures because of moist problems. Control of the power supplies is generally much easier than control of temperature. So for control of the intrinsic performance of an IC, changing $V_{DD}$ is much the easiest. For this reason the plot shown in figure 2, is the most commonly used in the industry. This is a Shmoo plot of $V_{DD}$ v Period, i.e. intrinsic capabilities v the extrinsic performance driven by timing. However, what Shmoo plotting can tell you about the performance of an IC is really only limited by your creativity. A Shmoo plot can tell you anything you wish to know, a few things you don’t, and can deceive you if you don’t watch out.

4 Future of Shmoo in Deep Sub-micron CMOS Technology

Technology trends seem to indicate that Shmoo plotting is going to be more important in the deep sub-micron era. By not scaling $V_{DD}$ with feature size, the excellent properties of the micron scale MOSFET have been retained in sub-micron devices in the last five years. This is changing as MOSFETs are scaled below 0.5 micron which requires $V_{DD}$ to be continuously scaled in future generations of deep sub-micron CMOS technologies. A particular issue is the control of the MOSFET threshold voltage. Smaller device dimensions coupled with larger wafer size makes spatial control of threshold voltage more difficult. However, with lower $V_{DD}$, the performance of the device becomes more dependent on the more complex characteristics of the MOSFET closer to the threshold voltage. Another issue in deep sub-micron CMOS is the problem of clock distribution. Clock distribution is the major analog design hurdle in the design of modern digital ICs, and problems in performance are frequently related to poor clock system design.

![Figure 2: VDD v Period Shmoo Plot](image-url)