Analog AC Harmonic Method for Detecting Solder Opens

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Abstract: Vectorless test techniques are attractive methods to quickly and inexpensively identify and diagnose common process related defects on manufacturers’ printed wiring boards. Junction Xpress is a new AC method developed to locate open and marginal solder connections without the use of digital vectors or overclamp style capacitive probes. Measuring response harmonics rather than simply the fundamental AC response reduces the tendency of false accepts of open connections.

Description: Analog harmonic test (AHT) is a vectorless technique for identifying and diagnosing solder related defects including open connections and marginal connections which exhibit resistance values greater than 20 to 50 ohms. AHT can also readily detect open bond wire connections inside integrated circuit packages and can determine whether the IC device is mis-oriented or completely missing.

AHT operates by applying a DC biased AC signal to one device pin on a semiconductor device and detecting the effects of the applied signal on another pin of the same device. The applied AC test signal typically passes through the device under test (DUT) electro-static protection diodes (ESD) or parasitic P-N structures and returns through the die substrate resistance.

The detector pin which is brought into conduction by a DC bias supplies an AC signal path from the modulated substrate to an external digitizing meter. The response spectrum is then processed by both continuous time and discrete time filters for increased frequency selectivity and rejection of noise. Open or marginal solder connections are identified by comparing the harmonic output spectrum from each device lead against pre-determined values.

The response harmonics are generated by the square law characteristics of the internal DUT parasitic substrate and protection P-N junctions. The relevance of examining the harmonic response components rather than simply the fundamental response is to minimize the possibility of “false passes” which would allow open pins to escape to the next level of product processing. More specifically, although the applied fundamental test signal may capacitively or conductively couple to the detector by alternate PWB paths, the harmonics are present in the response spectrum if there is a connective path between the instrument source and detector through one or more non-linear P-N junctions within the device under test.

Selecting optimal pin pairs for a single UUT connection test involves several steps. The circuit description file, or net list, is first analyzed to determine which pin pair candidates do not connect to another common device. This requirement is commonly met on most circuit assemblies. Secondly, fanout to other devices on the PWB is evaluated. The AHT software algorithm favors detector pins which have the fewest connected devices.

During a “learn mode” with one or more “golden boards”, pin pairs are then graded by maximum signal response, measurement standard deviation and by maximum spread between connected measurement and predicted open measurement. Open measurement readings are estimated by moving the AC source to other interconnected devices on the PWB and measuring the “background” readings with the detector. This technique has been proven to closely approximate what an open pin or connection would actually measure.

The AHT algorithm sources the pin being tested and attempts to find at least two possible detector pins. This secondary detector pin is used as an alternate detector should the primary detector pin be open.

Limitations: All vectorless tests have limitations and may need to be used in combination with other test methods to yield the desired fault coverage. Although AHT is a package insensitive vectorless technique and can test ball grid array (BGA) and flip chip devices, AHT does not perform well with devices containing internal dielectric isolation or with devices in highly parallel arrays that do not have at least one unique, non-bussed pin per device.