Introduction. SMT manufacturing created a sudden shift in fault spectrum making open solder joints the number one problem for many manufacturers. This problem was exacerbated by SMT ASIC’s and short life-cycle SMT VLSI devices for which power-on testing demanded difficult and time consuming test development. The only option to power-on in-circuit testing was power-on functional testing which lacks pin-level diagnostics. Population of both sides of the printed circuit board (PCB) further complicated both fixturing and measurement system solutions.

The development of SMT polarized capacitors and SMT connectors made visual inspection for correct orientation and connection virtually impossible. Undetected misoriented capacitors usually fail, and usually only after several hours of operation. Failures, often detected by consumers, frequently damage the attached PCB beyond repair. Open connectors create functional test diagnostic challenges.

Research and development leading to capacitive lead-frame testing began in the mid-1980’s. Parasitic diode detection techniques and parasitic transistor detection techniques led to the identification of parasitic capacitance that can be created on the metalization (lead frame) of IC’s, as well as connectors, some switches and capacitors. These parasitic capacitors proved very predictable and reliable. Removal of measurement system variability and topology-induced variability provided the test stability required for high volume manufacturing.

Open Solder Detection. The fundamental principal of this technique relies on the ability to discriminate between measurements made on good solder connections and open solder connections on either side of the PCB. The information generally required to detect solder shorts is all that is required for capacitive leadframe test generation. Most tests require no debug, and those that do are predictable.

As capacitors are created with two conductors separated by an insulator such as air, connectors and some switches (again metalization) are easily tested with the same fixturing probes and measurement technique used for digital and analog IC’s.

Fixturing and Throughput. This technique requires a unique fixturing implementation to create a capacitance between the measurement system and the device under test. Simple PCB’s plated on both sides (probes) are positioned over each device under test. Signal conditioning circuits are attached to this PCB to minimize noise and allow testing on both sides of the PCB. Throughput is a function of relay closure time, settling time and measurement time. Typical test time is in the order of 500 pins per second.

Benefits and Limitations. This technique makes well characterized measurements requiring no programming and little or no debug of digital, analog or mixed-signal IC’s and connectors. IC’s with ungrounded heatsinks are testable. IC’s with internal ground planes are typically untestable (internal circuitry above the ground plane is testable). Also untestable is the internal integrity of IC’s including bond wire attachment and silicon integrity. A natural extension of this technique is the measurement of the capacitance difference between the metalization (can) of a polarized capacitor and its internal composition. Additional measurements extend the measurement range into the range of capacitors and parallel capacitor combinations typically found on circuit topologies today.

Summary. Reliable pin-level diagnosis of open solder joints allows manufacturers to tune SMT process for maximum output. Repair time and repair-induced damage are both significantly reduced with pin-level diagnostics. Detection of misoriented capacitors prevents expensive and reputation-damaging field failures. Ability to test both sides of PCB’s allows maximum fault coverage.