CALL FOR PAPERS

ISQED 2009, 10th International Symposium on

QUALITY ELECTRONIC DESIGN

March 23-25, 2009. San Jose, CA, USA

The International Symposium on Quality Electronic Design (ISQED) is the leading Electronic Design & Design Automation conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting over 100 technical presentations, several keynote speakers, panel discussions, workshops/tutorials and other informal meetings. Conference proceedings are published by IEEE and posted in the digital library. Proceedings CD ROMs are published by ACM. In addition, continuing the tradition of reaching a wider readership in the IC design community, ISQED will continue to publish special issues in leading journals. The authors of high quality papers will be invited to submit an extended version of their papers for the special IEEE journal issues, such as TCAD, etc.

Papers are requested in the following areas

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers related to the manufacturing, design and EDA. Authors are invited to submit papers in the various disciplines of high level design, circuit design (digital, analog, mixed-signal, RF), test & verification, design automation tools; processes; flows, device modeling, semiconductor technology, and advance packaging. The details of various topics of paper submission are as follows:

- **Design for Manufacturability/Yield & Quality (DFM/DFY/DFQ)**
  - DFM/DFY/DFQ definitions, methodologies, matrices, and standards. Quality-based design methodologies and flows for custom, semi-custom, ASIC, FPGA, RF, memory, networking circuit, etc. Design flows and methodologies for SoC, and SiP. Analysis, modeling, and abstraction of manufacturing process parameters and effects for highly predictable silicon performance. Design and synthesis of ICs considering factors such as: signal integrity, transmission line effects, OPC, phase shifting, and sub-wavelength lithography, manufacturing yield and technology capability. Design for diagnosability, defect detection and tolerance; self-diagnosis, calibration and repair. Design and manufacturability issues for Digital, analog, mixed signal, RF, MEMS, opto-electronic, biochemical-electronic, and nanotechnology based ICs. Redundancy and other yield improving techniques. Global, social, and economic implications of design quality.

- **Physical Design, Methodologies & Tools (PDM)**
  - Physical design for manufacturing: Physical synthesis flows for correct-by-construction quality silicon, implementation of large SoC designs. Tool frameworks and data-models for tightly integrated incremental synthesis, placement, routing, timing analysis and verification. Placement, optimization, and routing techniques for noise sensitivity reduction and fixing. Algorithms and flows for harnessing crosstalk-delay during physical synthesis. Tool flows and techniques for antenna rule and electromigration rule avoidance and fixing. Spare-cell strategies for ECO, decoupling capacitance and antenna rule fixing. Physical planning tools for predictable power-aware circuits. Reliable clock tree generation and clock distribution methodologies for Gigahertz designs. EDA tools, design techniques, and methodologies, dealing with issues such as: timing closure, R, L, C extraction, ground/Vdd bounce, signal noise/cross-talk /substrate noise, voltage drop, power rail integrity, electromigration, hot carriers, EOS/ESD, plasma induced damage and other yield limiting effects, high frequency effects, thermal effects, power estimation, EMI/EMC, proximity correction & phase shift methods, verification (layout, circuit, function, etc.).

- **Design Verification and Design for Testability (DV/DFT)**
  - Hardware and Software, Formal and simulation based design verification techniques to ensure the functional correctness of hardware early in the design cycle. DFT and BIST for digital and SoC. DFT for analog/mixed-signal ICs and systems-on-chip, DFT/BIST for memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies. Design methodologies dealing with the link between testability and manufacturing.

- **EDA Methodologies, Tools, Flows & IP Cores; Interoperability and Reuse (EDA)**
  - EDA tools addressing design for manufacturing, yield, and reliability. Management of design process, design flows and design databases. EDA tools interoperability issues and implications. Effect of emerging technologies, processes & devices on design flows, tools, and tool interoperability. Emerging EDA standards. EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. IP modeling and abstraction. Design and maintenance of technology independent hard and soft IP blocks. Methods and tools for analysis, comparison and qualification of libraries and hard IP blocks. Challenges and solutions of the integration, testing, qualifying, and manufacturing of IP blocks from multiple vendors. Third party testing of IP blocks. Risk management of IP reuse. IP authoring tools and methodologies.

- **Robust & Power-conscious Devices, Interconnects, and Circuits (RDIC)**
  - Device, substrate, interconnect, circuit, and IP block modeling and simulation techniques; CMOS, Bipolar, and SiGe HBTs device modeling in the context of advanced digital, RF and high-speed circuits. Modeling and simulation of novel device and interconnect concepts. Signal integrity analysis: coupling, inductive and charge sharing noise; noise avoidance techniques. Modeling statistical process variations to improve design margin and robustness, use of statistical circuit simulators. Power grid design, analysis and optimization; timing analysis and optimization; thermal analysis and design techniques for thermal management. Power-conscious design methodologies and tools: low power devices, circuits and systems; power-aware computing and communication; power optimization and management. Design techniques for leakage current management. Design of robust 3D Integr
Submission of Papers

Paper submission must be done on-line through the conference web site at www.isqed.org. The guidelines for the final paper format are provided on the conference web site. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages) along with an abstract of about 200 words. To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. Please check the as-printed appearance of your paper before sending your paper. In case of any problems email isqed@isqed.org. Please note the following important dates:

<table>
<thead>
<tr>
<th>Paper Submission Deadline</th>
<th>September 30, 2008</th>
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<tbody>
<tr>
<td>Acceptance Notifications</td>
<td>November 23, 2008</td>
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<tr>
<td>Final Camera-Ready paper</td>
<td>January 3, 2009</td>
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