We will mainly address here the “alter ego” of quality, which is reliability, and is becoming a growing concern for designers using the latest technologies. After the DFM nodes in 90nm and 65nm, we are entering the DFR area, or Design For Reliability straddling from 65nm to 45nm and beyond. Because of the randomness character of reliability - failures can happen anytime anywhere - executives should mitigate reliability problems in terms of risk, which costs include cost of recalls, warranty costs, and loss of goodwill.

Taking as an example the soft error phenomenon, we demonstrate how the industry first started to respond to this new technology scaling problem with silicon test to measure and understand the issue, but should quickly move to resolving reliability issues early in the design. In this field, designers can largely benefit from new EDA analysis tools and specific IPs to overcome in a timely and economical manner this new hurdle.

**About Marc Derbey**

Marc Derbey was appointed CEO of iRoC Technologies in March 2006. Previously, he served as General Manager for European Operations where he managed all engineering efforts for both Operations and R&D. Marc sees his new position as CEO as a challenge to improve operating efficiency and build a strong team with both technical and commercial abilities. Marc has over 15 years experience in the software industry, managing service and software development teams for various multinational companies. He came to iRoC Technologies from Sun Microsystems where he was in charge of the Telco high availability software product development team. Prior to Sun Microsystems, Marc was senior manager at Bull SA where he was in charge of telecom software developments, and AIX kernel developments for NUMA technology. Marc holds a B.S in Computer Science for the Joseph Fourier University of Grenoble, an M.S in Artificial Intelligence from the Paul Sabatier University of Toulouse, and is certified from the Program Management Institute.