ISQED’07 TUTORIALS

Monday March 26
9:00am-5:00pm

Chair & Moderator
Rajiv Joshi
IBM

The tutorial session is constructed as a single full day tutorial track exploring important critical issues related emerging technologies, low power for sub-45 nm technologies and DFT, DFM analysis and power aware issues for SOC. The morning session includes topics such as emerging technologies, low power issues and self adaptive circuit techniques. The afternoon session discusses DFM, DFY, DFT and power aware designs of SOC.
Multi-Gate MOSFET Design

Presenter:
Gerhard Knoblinger, Infineon Technologies

Multi-Gate Field Effect Transistors (MuGFET) such as FinFETs and Triple-Gate FETs are the most promising device structures for sub-45nm CMOS technology nodes. The superior control of the channel due to multiple gates reduces short-channel effects and leakage currents. This opens the opportunity for further down scaling of the threshold and supply voltages and device performance improvements. Circuit performance also benefits from novel gate stack materials, reduced parasitic capacitances, and hole mobility improvement. For future SoC solutions in these advanced technologies, the ability to realize also analog building blocks is of utmost importance. In this tutorial, circuit design issues of emerging multi-gate field effect transistors will be discussed with special emphasis on the link between circuit design and technology. The tutorial will start with CMOS scaling trends, followed by an example for a typical MuGFET technology and an overview of the available devices. Reliable and accurate compact models for MuGFET devices, including new device specific effects are an important prerequisite for successful circuit design. So the second part will cover compact modeling of MuGFET devices with special emphasis on self heating effects. We will then discuss the impact of different technology options on the performance of digital circuits. The influence of novel midgap gate electrode materials on digital circuits will be presented. To compare different technology options, ring oscillator circuits are first realized with double gate devices using conventional body doping and n+/p+ poly-Si gates to define the nMOS/pMOS threshold voltages. To meet the requirements of future low power technologies, these circuits are then fabricated with triple gate devices and single-midgap gate electrodes allowing for enhancement-type devices with undoped bodies. Furthermore the influence of new device specific effects on analog circuits, like self heating or output conductance improvement due to undoped body are discussed and the first analog building blocks realized with MuGFET devices are presented. In addition RF and ESD issues will be discussed and RF circuits realized with MuGFET devices and the most important issues of ESD robustness will be covered.