There is one universal truth in terms of design for manufacturing (DFM)--DFM tools and disciplines have always existed. In micron technologies, manufacturing constraints were captured in process technology rule files. This process information was accessed at different levels of abstraction during various stages in the design flow. In addition, design teams implemented best practice methodologies and ‘experience-based’ guidelines throughout the design chain to ensure acceptable yield and adequate test coverage.

So what changed in the quest for an optimum DFM methodology? Nanometer technology has ushered in new and significant yield and manufacturing considerations and constraints. The lack of major increase in yield improvement between the 350nm and 180nm nodes suggests that the yield loss mechanisms are not only increasing in numbers, magnitude, and complexity at each successive generation, but they are increasing at a rate fast enough to largely offset ‘cosmetic’ improvements in tools and methodologies. If EDA tools are to assist the semiconductor industry at the 90nm and 65nm nodes, there must be profound changes to existing tools, and the introduction of new technologies that allow designers to consider and optimize for manufacturing at each stage of the design, verification, tapeout and test process. Where will these new tools and capabilities appear? They will show up in all parts of the design flow, as well as on the manufacturing floor. In particular, an immediate focus for the EDA industry must center on delivering new technology in four key areas: process modeling (electrical and lithographic), statistical analysis and visualization, design optimization and Test and inspection.

About Joe Sawicki

Joe Sawicki is the vice president and general manager of the Design-to-Silicon division, responsible for the Calibre design-to-silicon platform including physical verification, parasitic extraction, resolution enhancement, mask data preparation (MDP) and design for manufacturability (DFM) products. After eight years as an IC designer, Joe joined Mentor Graphics, where for 13 years he has held positions in Applications Engineering, Sales, Marketing and Management. He holds a BSEE from the University of Rochester and an MBA from Northeastern University’s High Technology Program.