Call for Papers

ISQED 2005
6th International Symposium on
QUALITY ELECTRONIC DESIGN

March 21-23, 2005
DoubleTree Hotel, San Jose, CA, USA

ISQED is the leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two-three panel discussions, workshops/tutorials and other informal meetings. Conference proceedings are published by IEEE Computer Society and hosted in the digital library. Proceedings CD ROMs are published by ACM.

Papers are requested in the following areas

Design for Manufacturability & Quality (DFMQ)
Analysis, modeling, and abstraction of manufacturing process parameters and effects for highly predictable silicon performance. Design and synthesis of high complexity ICs: signal integrity, transmission line effects, OPC, phase shifting, and sub-wavelength lithography, manufacturing yield and technology capability. Design for diagnosability, defect detection and tolerance; self-diagnosis, calibration and repair. Design and manufacturability issues for Digital, analog, mixed signal, RF, MEMS, opto-electronic, biocompactronics, and nanotechnology based ICs. Redundancy and other yield improving techniques. Design quality definitions and standards; design quality metrics to track and assess the quality of electronic circuit design, as well as the quality of the design process itself; design quality assurance techniques. Global, social, and economic implications of design quality. Design metrics, methodologies and flows for custom, semi-custom, ASIC, FPGA, RF, memory, networking circuit, etc. with emphasis on quality. Design metrics and quality standards for SoC, and SIP.

Package - Design Interactions & Co-Design (PDI)
Concurrent circuit and package design and effect on quality. Packaging electrical and thermal modeling and simulation for improved quality of product. SoC versus system in a package (SIP): design and technology solutions and tradeoffs; MCM and other packaging techniques; heat sink technology.

Design Verification and Design for Testability (DVFT)
Hardware and Software, formal and simulation based design verification techniques to ensure the functional correctness of hardware early in the design cycle. DFT and BIST for digital and SoC. DFT for analog/mixed-signal ICs and systems-on-chip, DFT/BIST for memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies.

Robust Device, Interconnect, and Circuits (RDIC)
Device, substrate, interconnect, circuit, and IP block modeling and simulation techniques; quality metrics, model order reduction; CMOS, Bipolar, and SiGe HBTs device modeling in the context of advanced digital, RF and high-speed circuits. Modeling and simulation of novel device and interconnect concepts. Signal integrity analysis: coupling, inductive and charge sharing noise; noise avoidance techniques. Power grid design, analysis and optimization; timing analysis and optimization; thermal analysis and design techniques for thermal management. Modeling statistical process variations to improve design margin and robustness, use of statistical circuit simulators. Power-conscious design methodologies and tools; low power devices, circuits and systems; power-aware computing and communication; system-level power optimization and management. Design techniques for leakage current management.

EDA Tools & IP Blocks; Interoperability and Implications (EDA)
EDA tools addressing design quality. EDA tools interoperability issues and implications. Management of design process, and design database. Effect of emerging processes & devices on design flows, tools, and tool interoperability. Emerging EDA standards. EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. Tools and methods for comparison of libraries and hard IP blocks. Challenges and solutions of the integration, testing, and qualifying of multiple IP blocks. IP authoring tools and methodologies. Methods and tools for design and maintenance of technology independent hard and soft IP blocks. IP modeling and abstraction. Risk management of IP reuse. Third party testing of IP blocks.
Submission of Papers

Three PDF files are required from authors; i) the full-length manuscript ii) the 200 words abstract and iii) a cover letter. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages) along with an abstract of about 200 words. To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. Include the complete contact author information in a separate file (cover letter). Cover letter must include:

I. Title of the paper
II. Name, affiliation, complete mailing address and phone, fax, and email of the first author
III. Name, affiliations, city, state, country of additional authors
IV. Person to whom correspondence should be sent, if other than the 1st author
V. Identification as invited paper if applicable
VI. Suggested area (as listed in previous page)

The guidelines for the final paper format is provided on the conference web site at www.isqed.org. Electronic submission via e-mail is the only accepted submission mode. Please email your paper in Adobe PDF format to publication@isqed.org. Please check the as-printed appearance of your paper before sending your paper. Please note the following important dates:

- **Paper Submission Deadline**: September 25, 2004
- **Acceptance Notifications**: November 1, 2004
- **Final Camera-Ready paper**: December 15, 2004

About ISQED

The International Symposium on Quality Electronic Design (ISQED), is a premier Design & Design Automation conference, aimed at bridging the gap between and integration of, electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues front-to-back. The conference provides a forum to present and exchange ideas and to promote the research, development, and application of design techniques & methods, design processes, and EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. The conference attendees are primarily designers of the VLSI circuits & systems (IP & SoC), those involved in the research, development, and application of EDA/CAD Tools & design flows, process/device technologists, and semiconductor manufacturing specialists including equipment vendors. ISQED emphasizes a holistic approach toward design quality and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities.