Call for Papers

ISQED 2004
5th International Symposium on
QUALITY ELECTRONIC DESIGN
March 22-24, 2004
San Jose, CA, USA

The International Symposium on Quality Electronic Design (ISQED), is a premier Design & Design Automation conference, aimed at bridging the gap between and integration of, electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. The conference provides a forum to present and exchange ideas and to promote the research, development, and application of design techniques & methods, design processes, and EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. The conference attendees are primarily designers of the VLSI circuits & systems (IP & SoC), those involved in the research, development, and application of EDA/CAD Tools & design flows, process/device technologists, and semiconductor manufacturing specialists including equipment vendors. ISQED emphasizes a holistic approach toward design quality and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities.

Conference Highlights

Keynote presentations by prominent experts & leaders

**Invited papers on key aspects of Design, EDA, and Semiconductor Technology**

Panels discussing hot issues of general interest such as SoC, Design Closure, Interoperability, and Technology trends

Best Paper Awards

**Tutorial and Workshop tracks exploring many aspects of logical & physical design, design for testability, and design for manufacturability**

Important Dates

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<tr>
<td>Paper Submission Deadline</td>
<td>September 15, 2003</td>
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<td>Acceptance Notification</td>
<td>November 1, 2003</td>
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www.isqed.org
With Technical sponsorship of
IEEE Electron Device Society (EDS),
IEEE Components, Packaging, & Manufacturing Technology Society (CPMT), and in cooperation with ACM/sigDA, and FSA
Papers are requested in the following areas

**Design for Manufacturability (DFM)**
Analysis, modeling, and abstraction of manufacturing process parameters and effects for highly predictable silicon performance. Design and synthesis of high complexity ICs: signal integrity, transmission line effects, OPC, phase shifting, and sub-wavelength lithography; manufacturing yield and technology capability. Design for diagnosability, defect detection and tolerance; self-diagnosis, calibration and repair. Design and manufacturability issues for analog, mixed signal, MEMS, opto-electronic and biochemical-electronic ICs; design and manufacturing issues for nano-technology based ICs. Redundancy and other yield improving techniques.

**Methodologies and Metrics for Design Quality (MDQ)**
Design quality definitions and standards; design quality metrics to track and assess the quality of electronic circuit design, as well as the quality of the design process itself; design quality assurance techniques. Global, social, and economic implications of design quality. Design metrics, methodologies and flows for custom, semi-custom, ASCIC, FPGA, RF, memory, networking circuit, etc. with emphasis on quality. Design metrics and quality standards for SoC, and SIP.

**Package - Design Interactions & Co-Design (PDI)**
Packaging electrical and thermal modeling and simulation for improved quality of product. SoC versus system in a package (SiP): design and technology solutions and tradeoffs; MCM and other packaging techniques; heat sink technology. Concurrent circuit and package design and effect on quality.

**Design for Testability (DFT)**
DFT and BIST, DFT for analog/mixed-signal ICs and systems-on-chip, DFT/BIST for memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies.

**Device, Interconnect and Circuit Level Modeling and Analysis (DEV)**
Device, substrate, interconnect, circuit, and IP block modeling and simulation techniques; quality metrics, model order reduction; SiGe HBTs and CMOS device modeling in the context of RF and high-speed circuits. Modeling and simulation of novel device and interconnect concepts such as single electron transistors (SET), hybrid SET-FET architectures, 3-D ICs, optical interconnects, etc. Signal integrity analysis: coupling, inductive and charge sharing noise; noise avoidance techniques. Power grid design, analysis and optimization; timing analysis and optimization; thermal analysis and design techniques for thermal management. Modeling statistical process variations to improve design margin and robustness, use of statistical circuit simulators.

**EDA Tools, Interoperability and Implications (EDA)**
EDA tools addressing design quality. EDA tools interoperability issues and implications. Management of design process, and design database. Effect of emerging processes & devices on design flows, tools, and tool interoperability. Emerging EDA standards, EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits.

**Low Power Design and Test (LPD)**

**Physical Design, Methodologies & Tools (PDM)**
Physical synthesis flows for correct-by-construction quality silicon, implementation of large SoC designs. Tool frameworks and datamodels for tightly integrated incremental synthesis, placement, routing, timing analysis and verification. Placement, optimization, and routing techniques for noise sensitivity reduction and fixing. Algorithms and flows for harnessing crosstalk-delay during physical synthesis. Tool flows and techniques for antenna rule and electromigration rule avoidance and fixing. Spare-cell strategies for ECO, decoupling capacitance and antenna rule fixing. Planning tools for predictable high-current, low-voltage power distribution. Reliable clock tree generation and clock distribution methodologies for Gigahertz designs. EDA tools, design techniques, and methodologies, dealing with issues such as: timing closure, R, L, C extraction, ground/Vdd bounce, signal noise/crosstalk /substrate noise, voltage drop, power rail integrity, electromigration, hot carriers, EOS/ESD, plasma induced damage and other yield limiting effects, high frequency effects, thermal effects, power estimation, EMI/EMC, proximity correction & phase shift methods, verification (layout, circuit, function, etc.), packaging modeling and simulations.

**Design and Abstraction Methods for SoCs, IP Blocks and Libraries (SIL)**
Tools and methods for comparison of libraries and hard IP blocks. Challenges and solutions of the integration, testing, and qualifying of multiple IP blocks. IP authoring tools and methodologies. Methods and tools for design and maintenance of technology independent hard and soft IP blocks. IP modeling and abstraction. Risk management of IP reuse. Third party testing of IP blocks.

**Effects of Technology on IC Design, Performance, Reliability, and Yield (TRD)**
Emerging issues in DSM CMOS: e.g. sub-threshold leakage, gate leakage, technology road mapping and technology extrapolation techniques. New technologies such as SOI, Double-Gate(DG)-MOSFET, Gate-All-Around (GAA)-MOSFET, Vertical-MOSFET, strained CMOS, high-bandwidth metallization, etc. Challenges of mixed-signal design in digital CMOS or BiCMOS technology, including issues of substrate coupling, cross-talk and power supply noise. Significance of reliability effects such as gate oxide integrity, electromigration, ESD, etc., in relation to electronic design. Impacts of process technologies on circuit design and capabilities (e.g. low-Vt transistors versus increased off-state leakage) and the accuracy, use and implementation of SPICE models that faithfully reflect process technologies, lessor applications of TCAD to circuit design.
Submission of Papers

Three PDF files are required from authors; i) the full-length manuscript ii) the 200 words abstract and iii) a cover letter. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages) along with an abstract of about 200 words. To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. Include the complete contact author information in a separate file (cover letter). Cover letter must include:

I. Title of the paper
II. Name, affiliation, complete mailing address and phone, fax, and email of the first author
III. Name, affiliations, city, state, country of additional authors
IV. Person to whom correspondence should be sent, if other than the 1st author
V. Identification as invited paper if applicable
VI. Suggested area (as listed in previous page)

The guidelines for the final paper format is provided on the conference website at www.isqed.org. Electronic submission via e-mail is the only accepted submission mode. Please email your paper in Adobe PDF format to widerkehr@isqed.org. Please check the as-printed appearance of your paper before sending your paper. Please note the following important dates:

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Submission of Tutorial Proposals

Several tutorial sessions will be held on the first day, where presentations by many industry experts would offer valuable opportunities for practicing professionals to refresh or upgrade their skills in quality-based IC design techniques, methodologies and tools. Please send your proposals to the ISQED tutorial committee to widerkehr@isqed.org. The tutorial proposal should include:

- Title of Tutorial
- Name(s), address, and affiliation of the moderator
- Name(s), address, and affiliation of presenter(s)
- Half-page summary of each presenter’s biography

You may send your proposal by email as straight text or as an Adobe PDF file. All tutorial presentations should be technical, up to date, relevant, and target the design community. Marketing presentations will not be accepted. In order to meet the conference timeline, we would like to have your proposal no later than Sept. 22, 2003. Final version of the slides are due February 15, 2004.

Submission of Workshop Proposals

Several workshop sessions will be held on the last day of the conference. ISQED workshops are intended to supplement the conference by providing in-depth, practical and proven design solutions for practicing design professionals. Workshops will be taught by experts in the field, who are intimately involved with the issues and solutions in their perspective areas, from both the industry and academia. Please send your proposals to the ISQED workshop committee to widerkehr@isqed.org. The workshop proposal should include:

- Title of Workshop
- Name(s), address, and affiliation of the moderator
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