Tutorial D3
1:30pm-3:15pm

Quality Aspects of SOI Circuit Design

Organizer: Andrew Marshall, Texas Instruments, Inc.
Presenter: Andrew Marshall, Texas Instruments, Inc.

This tutorial focuses on challenges of SOI design and test. With the switch from bulk to SOI, combined with technology scaling, new issues are being raised about IC quality and reliability. Design and testing techniques for ICs built on SOI material are explained. This tutorial covers the following topics: Basic analog, digital and memory design techniques for SOI applications. Floating body effects. Differences between design of SOI and bulk – active and passive component performance. Low-voltage low-power SOI CMOS design style, Cross-talk and local heating issues, Simulation of SOI designs, layout techniques for SOI, Testing of SOI circuits to ensure quality product.

Tutorial D4
3:30pm-5:15pm

Optimization in an Integrated Physical Design Flow

Organizer: Olivier Coudert, Monterey Design Systems, Inc.
Presenter: Olivier Coudert, Monterey Design Systems, Inc.

The purpose of a physical design flow is to take a netlist with a set of constraints (timing, area, power, etc.), and to produce a production worthy layout. This cannot be achieved without considering all the interdependencies between placement, timing, logic optimization, routing, etc. Traditional optimization methods that have been used more or less independently: for example, placement optimization did not interact with logic optimization. Today’s need for integrated physical design flows requires these methods to be more “educated” about each other and to work simultaneously. This tutorial will present a physical design flow and describe how different optimization methods (placement, logic, routing) cooperate together.