Keynote Speech

A Utility-Based Routing Scheme and Its Applications

Jie Wu
Florida Atlantic University, USA

Abstract

To efficiently address the routing problem in dynamic network systems, we introduce a new utility metric, maximum expected social welfare, and integrate the cost and stability of nodes in a unified model to evaluate the optimality of routes. The expected social welfare is defined in terms of expected benefit (of the routing source) minus the expected costs incurred by forwarding nodes. Based on this new metric, we design an optimal and efficient algorithm, and implement the algorithm in both centralized (optimal) and distributed (near-optimal) manners. We also look at several extensions in improving benefit, all optimal routes, incentive compatible routing, and applications of this new model.

Prof. Jie Wu is a distinguished professor in the Department of Computer Science and Engineering, Florida Atlantic University. From 2006 to 2008, he served as a program director at US National Science Foundation. He has been on the editorial board of the IEEE Transactions on Parallel and Distributed Systems and was a guest editor of Computer and the Journal of Parallel and Distributed Computing. He is currently on the editorial board of the IEEE Transactions on Mobile Computing. He was a program cochair of the First IEEE International Conference on Mobile Ad Hoc and Sensory Systems (MASS 2004), the executive program vice chair of the 28th IEEE International Conference on Distributed Computing Systems (ICDCS 2008), and the program vice chair of the 29th International Conference on Parallel Processing (ICPP 2000). He was also the general chair of MASS 2006 and is the general chair of the 22nd IEEE International Parallel and Distributed Processing Symposium (IPDPS 2008). He has served as a distinguished visitor of the IEEE Computer Society and is the chairman of the IEEE Technical Committee on Distributed Processing (TCDP). His research interests include wireless networks and mobile computing, routing protocols, fault-tolerant computing, and interconnection networks. He has published more than 450 papers in various journals and conference proceedings. He is the author of Distributed System Design (CRC Press). He is the recipient of the 1996-1997, 2001-2002, and 2006-2007 Researcher of the Year Awards from Florida Atlantic University. He is a fellow of the IEEE.
Keynote Speech

Heterogeneous Parallel Architecture, Compilation and Programming

Xuejun Yang

National University of Defense Technology, China

Abstract

Using general processors and accelerators, such as stream processors and GPGPUs, to construct a heterogeneous system has become a hotspot in the research trend of large-scale parallel computing, for such systems can achieve very high performance/power ratio with relatively low power consumption and reduce system scale. We design and implement a 64-bit stream processor, Fei Teng 64 (FT64), which supports two kinds of communications, message passing and stream communications, based on which we design a heterogeneous system utilizing FT64 as the accelerator. We devise a novel stream programming language Stream FORTRAN95 (SF95), together with the compiler, SF95Compiler, so as to facilitate the development of scientific applications on the heterogeneous system. We also develop the corresponding compiling optimization technologies. We then propose the judging conditions to determine if a program could be streamized. We further propose one approach to exploit Loop-Dependent Stream Reuse for Stream processors and another for optimizing utilization of stream register files in stream processors based on Comparability Graph Coloring.

Prof. Xuejun Yang is a distinguished professor of Computer Science in China. He serves as the deputy director of National Laboratory for Parallel and Distributed Processing and is a trustee of China Computer Federation. He is also the director of China Computer Federation's Special Committee for Architecture and the vice director of its Special Committee for System Software. Yang is currently on the editorial board of Chinese Journal of Electronics and Journal of Computer Research and Development. He is the recipient of the National Science Foundation for Distinguished Young Scholars. His research group is funded by the Innovative Research Group Fund from Chinese National Natural Science Foundation, where Yang serves as the academic leader. Yang has been working on the architecture of High Performance Computers and forefront technologies of Parallel and Distributed Processors for more than twenty years. He is the general designer of YinHe series High Performance Computers. Yang's research results have been accepted by high-level international journals such as the IEEE Transaction on Parallel and Distributed Systems and the Journal of Supercomputing, and by high-level international conferences such as ISCA'07, PPOPP'09, PACT'07/08 and ICDCS'08.
Keynote Speech

High Performance Routers Using FPGAs

Viktor K. Prasanna
University of Southern California, USA

Abstract
Reconfigurable devices and systems have evolved dramatically over the past decade. Recently, several state-of-the-art high end platforms have incorporated FPGAs (Field Programmable Gate Arrays) for application acceleration including high end routers. This talk explores architectures and algorithms for accelerating core network functions including deep packet inspection and packet classification in Internet routers. We illustrate the performance improvements for such systems and demonstrate the suitability of FPGAs for these computations. We also propose energy efficient designs to realize the “Green Internet” vision. We show that SRAM based solutions combined with FPGA based architectures lead to high throughput as well as reduced power dissipation compared with the state of the art solutions based TCAMs. We conclude by highlighting the challenges in further exploiting this technology for such applications.

Prof. Viktor K. Prasanna (ceng.usc.edu/~prasanna) is Charles Lee Powell Chair in Engineering in the Ming Hsieh Department of Electrical Engineering and Professor of Computer Science at the University of Southern California. He is the executive director of the USC-Infosys Center for Advanced Software Technologies (CAST). He is also a member of the USC-Chevron Center of Excellence for Research and Academic Training on Interactive Smart Oilfield Technologies. His research interests include parallel and distributed systems including networked sensor systems, embedded systems, configurable architectures and high performance computing. He has served on the editorial boards of the Journal of Parallel and Distributed Computing, Proceedings of the IEEE, IEEE Transactions on VLSI Systems, and IEEE Transactions on Parallel and Distributed Systems. He served as the Editor-in-Chief of the IEEE Transactions on Computers during 2003-06. Prasanna was the founding Chair of the IEEE Computer Society Technical Committee on Parallel Processing. He is the steering chair of the IEEE International Conference on High Performance Computing (www.hipc.org). He is a Fellow of the IEEE and the ACM. He is a recipient of 2009 Outstanding Engineering Alumnus Award from the Pennsylvania State University.