Multiple Peak Resonant Tunneling Diode for Multi-Valued Memory *

Sen-Jung Wei and Hung-Chang Lin
Department of Electrical Engineering
University of Maryland
College Park, MD 20742

Abstract
Several designs are presented for a high speed static random access multi-valued memory using the folding characteristics of multiple peak Resonant Tunneling Diodes (RTDs). The different designs are described and studied by comparing their power consumption under different conditions of device parameters and the switching speed. This paper shows that the proposed memory cell using a pair of multiple peak RTDs yields the best result from the standpoint of size, power dissipation and speed.

1 Introduction
It is known that use of multi-valued logic circuits can provide more information for each signal line, and reduce the number of interconnections within a chip or between chips [1]. For this system, it is desirable to have a high-density and high-speed multi-valued static random-access-memory (SRAM) to perform the function of storage. To increase the density of the storage element to get 2 stable states. We have developed a multi-state memory cell, in which the number of memory states can increase to $2N+1$ for the same N-peak RTDs. In this paper, the static power dissipation and switching speed are compared to show the improvement of our new circuit. Sections 2, 3, and 4 describe the resistance load method, the constant current source load method and the RTD load method respectively. In section 5, the power consumption and switching speed are compared for different designs. The experimental results are demonstrated in section 6.

2 Resistance Load Method
When a resistor is connected as a load for the multiple peak RTD [6] (Fig. 2(a)), the load line can intersect with the positive resistance sections of the multiple peak RTD characteristics in several operating points ($P_1 \sim P_3$) as shown in Fig. 2(b). These multiple operating points represent multi-valued memory states. Any input write voltage between $V_1$ and $V_2$ will settle at operating point $P_1$, because the discharging current from the node capacitance by the multiple peak RTD is larger than the charging current from the resistive load, thus reducing the node voltage until equilibrium is reached at $P_1$. In similar fashion, any input write voltage between the intersecting voltages $V_2$ and $V_3$ sets at operating point $P_2$. For a resistive load, the supply voltage $V_{DD1}$ needs to be large, so the load line can intersect all the positive resistance regions of the multiple peak RTD. In the following calculations, we assume the negative differential resistance $|R_N|$ equal to zero (this is a practical assumption for multiple peak RTD and $|R_N|$ should be made as close to zero as possible to increase the switching speed). The bias currents of the three stable states are at $I_1$, $I_2$, and the supply voltage is $V_{DD1}$. For each stable state, the noise margin is defined as the minimum value of the difference between the bias current and the peak current ($I_P$), and the difference between the bias current and the valley current ($I_V$). In order to maximize the noise margin of the memory cell, $I_2$ is chosen equal to $\frac{I_P + I_V}{2}$, then the noise margins for $I_1$ and $I_2$ are equal. The supply voltage for this cell can be calculated as:

$$V_{DD1} = \frac{2I_1(I_P - I_V)R_P}{2I_1 - I_P - I_V} \quad (1)$$

where $R_P$ is the positive differential resistance for the multiple peak RTD. The power dissipation for this structure is:

$$P_{power(1)} = \frac{3R_P I_1(I_P - I_V)I_{L1}I_{L2}}{2I_P^2 - (1 + \frac{I_{L1}}{I_P})}$$
sipation for this circuit: 

\[ P_1 = \frac{3R_P I_P^2 \alpha(1 - \beta)(1 + \beta)}{2\alpha - 1 - \beta} \]

for \(0.5(1 + \beta) \leq \alpha \leq 1\) \( \text{(2)} \)

where \(\alpha = \frac{I_P}{I_c}\), \(\beta = \frac{I_c}{I_p}\). By dividing \(P_{\text{power(1)}}\) by \(3R_P I_P^2\), one obtains the normalized average power dissipation for this circuit:

\[ P = \frac{\alpha(1 - \beta)(1 + \beta)}{(2\alpha - 1 - \beta)} \]

for \(0.5(1 + \beta) \leq \alpha \leq 1\) \( \text{(3)} \)

The normalized noise margin for this circuit is \(\frac{I_c - I_p}{I_c + I_p} = \frac{1 - \beta}{1 + \beta}\).

### 3 Constant Current Source Load Method

The supply voltage can be reduced if the resistance load is replaced by a current source. Fig. 3(a) is the circuit for the memory cell biased by a current source \(I_L\). The I-V characteristic of the 2-peak RTD and the load line are shown in Fig. 3(b). For this circuit, the three bias currents: \(I_1\), \(I_2\) and \(I_3\) are at the same value. By assuming the differential resistance for the linear region of the current source device has the same value as that of the multiple peak RTD, one can calculate the supply voltage as:

\[ V_{DD3} = Rp(3I_P - 2I_L + I_1) \]

and the normalized average power dissipation is:

\[ P_2 = \alpha(\alpha + 3 - 2\beta) \]

for \(\beta \leq \alpha \leq 1\) \( \text{(5)} \)

where \(\alpha = \frac{I_P}{I_c}\), \(\beta = \frac{I_c}{I_p}\). The normalized noise margin for this cell is the minimum value of \(\frac{1 - \beta}{1 + \beta}\) and \(\frac{\alpha - \beta}{1 - \beta}\). As can be seen later, the normalized noise margin is much larger than that for the resistance load method for the same power dissipation.

### 4 RTD Load Method

The proposed multi-valued SRAM cell is shown in Fig. 4(a), where the two multiple peak RTDs with resistors in series constitute the storage element. When a multiple peak RTD with symmetrical positive and negative resistance, as shown in Fig. 4(b) curve a, is connected in series with a resistor, the resultant folding characteristic becomes unsymmetrical, as shown in Fig. 4(b) curve b. With a resistor in series, the differential resistance of the positive region increases and the magnitude of the differential resistance of the negative region decreases. The operational characteristics can be easily explained by the current continuity and the KVL laws \([9]\). There are at least two modes of operation for this storage element depending on the supply voltage and the \(\frac{I_P}{I_c}\) ratio of the I-V characteristics of multiple peak RTDs. Fig. 5(a) shows the case of three stable states for a 2-peak RTD pair, which can be considered as the extension of the Goto pair \([8]\). By properly choosing the supply voltage and the series resistors, one can get five stable states for a 2-peak RTD pair as shown in Fig. 5(b). The basic principle of operation of this memory cell can be explained with reference to Fig. 4(a). The selection switch is controlled by the address busses. A read operation is performed by enabling the selection switch, which selects a particular cell, and enabling the read switch. The state of this cell is then sensed by a sense amplifier. A write operation is performed by enabling the selection and write switches. The state of this selected cell will be changed to the multi-valued digital data input.

Fig. 6(a) is the circuit for the proposed storage element and Fig. 6(b) is the I-V characteristic of the multiple peak RTD and the RTD load line for the three-stable state case. The supply voltage is:

\[ V_{DD3} = Rp(I_P - I_L + 2I_1) \]

and the normalized average power dissipation is:

\[ P_3 = 2(\alpha + 0.5 - 0.5\beta)(3\alpha + 0.5 - 0.5\beta)/3 \]

for \(\beta \leq \alpha \leq 0.5(1 + \beta)\) \( \text{(7)} \)

where \(\alpha = \frac{I_P}{I_c}\), \(\beta = \frac{I_c}{I_P}\). Fig. 6(c) is the I-V characteristic for the multiple peak RTD with the load line for the 5-stable states case. The supply voltage is:

\[ V_{DD4} = 2Rp(I_P - I_L + I_1) \]

and the normalized average power dissipation is:

\[ P_4 = 0.4(\alpha + 1.0 - \beta)(5\alpha + 1.0 - \beta) \]

for \(\beta \leq \alpha \leq 0.5(1 + \beta)\) \( \text{(9)} \)

where \(\alpha = \frac{I_P}{I_c}\), \(\beta = \frac{I_c}{I_P}\). The normalized noise margin for this cell is the minimum value of \(\frac{\alpha - \beta}{1 - \beta}\) and \(\frac{1 - \beta}{1 + \beta}\).

### 5 Power Consumption and Switching Speed Comparisons

Fig. 7(a) shows the normalized average power dissipation as a function of the normalized noise margin for different circuit structures when \(\frac{I_P}{I_c} = 3.0\). For the same noise margin, the circuit with a resistor load has the largest power dissipation and the circuit with the RTD load has the smallest power dissipation assuming equal numbers of states for each cell. The maximum noise margin for the nonlinear bias method is half of the other circuit structures. For typical multiple peak RTD I-V characteristic, this is not a disadvantage if one takes the speed response into account and carefully designs the device structure and the circuit. As a quantitative example for the power saving of the multiple peak RTD load method when the normalized noise margin equal to 0.25: \(P_3\) is 45% of \(P_1\) and
71% of $P_2$. Fig. 7(b) shows the case when $k = 10.0$; the power dissipations for all the circuit structures decrease as expected.

Fig. 8 shows the load lines with the I-V characteristic of multiple peak RTD of a three stable state memory cell for different bias methods: curve a is the load line for the constant current source load method, curve b is the load line for the constant current source load method, curve c is the load line for the RTD load method. From the figure, it can be seen that one drawback of the resistance load method is that the pull in range is unsymmetrical (pull in range means the voltage difference between that of the stable point and the unstable point, where the load line intersect the multiple peak RTD at the negative resistance regions), for each operating point. The speed of switching processes depends on the difference between the current of multiple peak RTD and the current coming from the load. If we assume the node voltage of the initial state is $V_i$ and that of the final state is $V_F$, then the current available for the switching process equals the triangle $XYZ$ for the constant current bias method and that for the RTD bias method equals the triangle $XZW$, which is about twice as large as triangle $XYZ$.

6 Experimental Results
A breadboard circuit (Fig. 9) has been implemented to verify the concept of the RTD load method. The five operating points at $V_1$, $V_2$, $V_3$, $V_4$, and $V_5$ represent the logic levels 0, 1, 2, 3, and 4. Whenever the write switch controlled by $C_n$ is on, the corresponding state $V_n$ is written into the storage element, where $1 \leq n \leq 5$. After the write cycle, the read switch is on to sense the state of the storage element. The timing diagram for the control signals is shown in Fig. 10, where $R$ is the control signal for the read switch, $C_n$ is the control signal for the write switch, where the $C_n$ and $R$ are nonoverlapping signals. Fig. 11 shows the experimental results of the test circuit. This is a single measurement. Because of the channel number limitation of the oscilloscope, three pictures were taken. The “Output Signal” and “R” are identical for three photos; different pairs of control signals are shown. The sensed voltages after the read switch are in the sequence of $1.5V$, $0.9V$, $1.2V$, $0.7V$, and $0.4V$—the same sequence as the write in clock. Therefore a 5-state SRAM cell is successful demonstrated by using a 2-peak RTD pair.

7 Conclusion
Different bias methods for the multi-valued RTD SRAM are described. By using another multiple peak RTD as the nonlinear load, the states number of the cell can be doubled and the bias voltage can be lowered. The power consumptions for different circuit structures are compared for different device parameters. For good noise margin, the proposed method can increase the packing density and reduce the power dissipation. The RTD bias method is easier to be integrated than either the resistance load or the current source load method, because it is not necessary to fabricate different devices on the same chip. The speed response for the proposed method can be improved due to the larger current difference between the load and the driver in the switching process.

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References

* U. S. Patent Pending
Fig. 1 I-V characteristic of a 5-peak RTD

Fig. 2(a) memory cell with resistor load
Fig. 2(b) I-V characteristic with resistor load line

Fig. 4(a) Proposed memory cell

Fig. 4(b) The effect of a resistor in series with the RTD; curve a: without resistor curve b: with resistor

Fig. 3(a) memory cell with constant current source load
Fig. 3(b) I-V characteristic with constant current source load line

Fig. 5(a) RTD pair with three stable states active load

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Fig. 5(b) RTD pair with five stable states

Fig. 6(a) memory cell with RTD load
Fig. 6(b) I-V curve with RTD load line having 3 states

Fig. 6(a) memory cell with RTD load
Fig. 6(c) I-V curve with RTD load line having 5 states

Fig. 7(a) normalized average power dissipation
Fig. 7(b) normalized noise margin

- Curve a: resistor load
- Curve b: current source load
- Curve c: RTD load 3 states
- Curve d: RTD load 5 states
Fig. 9 Test circuit

Fig. 10 Timing Diagram

Fig. 11 Experimental results of the test circuit