The Impact of Variability on Power

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ABSTRACT
The integrated circuit manufacturing process has inevitable imperfections and fluctuations that result in ever-growing systematic and random variations in the electrical parameters of active and passive devices fabricated. The impact of such variations on various aspects of chip performance has been the subject of numerous papers, and techniques for analyzing and dealing with such variability -broadly labelled design for manufacturability are emerging as the next hot topic in this area.

The focus of much of the current work in this area has been on timing, but it is well known that modern integrated circuits are very heavily power limited and that static and dynamic power have emerged as first class design objectives. In this paper, we review the various sources of process variability, and relate them to variability in the various parts of the power delivery subsystem. Specifically, we address variability in the following areas:

1. Static (leakage) power. This is the portion of the power dissipated in the integrated circuit which exists when the power is applied, but circuits are not operating. This part of the overall power problem has been receiving much attention recently since technology scaling has been causing a large increase in intrinsic device leakage.

2. Dynamic power. This is the power required to operate digital switching circuits such as buffers, latches, memory arrays and logic gates. The estimation of dynamic power has been the area of much research over the last 20 or so years. To a large degree, however, the impact of manufacturing variability in this area has not received much attention.

3. On-chip power grid. This takes into account variability in the integrated circuit wires and vias that constitute the chip power grid. Power grid wires encompass all metal levels (layers) in a design and often occupy 20 percent or more of the total wiring resources. The distributed nature of the power grid is intended to decrease its sensitivity to certain types of variation.

4. On-chip decoupling capacitance. This models the impact of variability on the various components of on-chip decoupling capacitance including both special-purpose decoupling capacitors as well as the so-called quiet capacitance associated with circuits which are not switching. This is a subject which has received very little attention, but is becoming crucial for high speed multi-GHz designs.

5. Package power grid. This includes the effect of tolerances and variations in the manufacture of the package. Since the package is manufactured using a process distinct from that of integrated circuit fabrication, the character of the variations is different.

6. Workload. One source of uncertainty in power delivery is lack of detailed knowledge of design operation. Some of this lack of detailed knowledge is due to the fact that power delivery systems (both on chip and package) are often designed concurrently with the design, leading to a lack of detailed placement information and power estimates for parts of the design. Nevertheless, this source of variability is important and needs to be considered along with the other more physical sources above.

It is important to model all these sources of variability with the correct balance of effort and accuracy, thus it is important to get broad bounds on each of the sources in order to insure that the appropriate level of modeling and analysis investment is made in order to bound or worst-case each component without undue pessimism.

It is also important to have a first order understanding of the technology trends in each of these sources of variability. This will allow the designer and CAD tool developer to anticipate future problem areas and plan work arounds as needed.