Directory-Based Cache Coherency Protocol for a Ring-Connected Multiprocessor-Array

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ABSTRACT

The main goal of this paper is to demonstrate that a multiprocessor with very fast point-to-point interconnection can be 10 times faster than a bus-based one. In this work, we presented a two-dimensional ring-connected system where the processing-nodes are arranged in rows and columns and interconnected through horizontal and vertical unidirectional 64-bit links (similar to the Illiac 4). After presenting the architecture for the processing-nodes, the pipelined feature of the network and the cache-coherency protocol, we discussed some implementation issues for the system. Using trace-driven simulation, some performance results for the new system and for a bus-based two-dimensional system (similar to the Wisconsin multicube) were presented to show the superiority of using point-to-point interconnections instead of busses.

Revisit The Case For Direct-Mapped Caches: A Case For Two-way Set-Associative Level-Two Caches

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ABSTRACT

In this paper we argue that a two-way second-level cache is a better design choice than a direct-mapped organization. We show two-way caches are as simple to implement as direct-mapped caches. If the cache controller contains tags, the data array can be organized as a single bank of standard SRAM. Otherwise, both tag and data can be organized as a single SRAM bank. Our simulation results show these novel two-way organizations outperform the direct-mapped approach.