Pipelining and Bypassing in a VLIW Processor

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ABSTRACT
This paper describes issues involved in the bypassing mechanism for a VLIW processor and its relation to the pipeline structure of the processor. We will first describe the pipeline structure of our processor and analyze its performance and compare it to typical RISC-style pipeline structures given the context of a processor with multiple functional units. Next, we shall study the performance effects of various bypassing schemes in terms of their effectiveness in resolving pipeline data hazards and their effect on the processor cycle time.

Synthesis of Application-Specific Heterogeneous Multiprocessor Systems

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ABSTRACT
Heterogeneous systems can achieve enhanced performance and/or cost-effectiveness over homogeneous systems. SOS, a formal method to synthesize optimal heterogeneous systems for given applications, involves creation and solution of a mixed integer-linear programming model. A primary component of the model is the set of relations to be satisfied to ensure proper ordering of various events in the task execution, and completeness and correctness of the system. Experiments indicate SOS can be useful in designing heterogeneous systems.