A New Compiler-Directed Cache Coherence Scheme for Shared Memory Multiprocessors with Fast and Parallel Explicit Invalidation

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ABSTRACT
We propose a novel compiler-directed cache management scheme which allows parallel invalidation of a subset of array elements. The scheme limits non-stale data invalidations using a novel memory allocation technique. Its correctness is proved using a flow graph model. It is also shown that the scheme provides more cacheability than the previous compiler-directed ones and has lower overhead in determining read hit at runtime. A new performance parameter called unwanted invalidation ratio, for compiler-directed coherence schemes is also proposed.

The Time-Constrained Barrier Synchronizer and its Applications in Parallel Systems

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ABSTRACT
A barrier synchronizer, allowing processors to participate dynamically by letting them register their intent to participate within a timeout period, is presented. The synchronizer allows some applications - like software combining and highly concurrent queue operations - to be implemented in a rather unconventional but highly efficient manner. The barrier synchronizer generates successive time windows, allowing requests within the same window to be combined, thus ensuring a more-or-less fixed latency for the Fetch-and-Op primitive.