A New Compiler-Directed Cache Coherence Scheme for Shared Memory Multiprocessors with Fast and Parallel Explicit Invalidation

Ahmed Louri Hongki Sung

Department of Electrical and Computer Engineering
University of Arizona
Tucson, AZ 85721
Email: louri@paris.ece.arizona.edu
(602) 621-2318

ABSTRACT

We propose a novel compiler-directed cache management scheme which allows parallel invalidation of a subset of array elements. The scheme limits non-stale data invalidations using a novel memory allocation technique. Its correctness is proved using a flow graph model. It is also shown that the scheme provides more cacheability than the previous compiler-directed ones and has lower overhead in determining read hit at runtime. A new performance parameter called unwanted invalidation ratio, for compiler-directed coherence schemes is also proposed.

The Time-Constrained Barrier Synchronizer and its Applications in Parallel Systems

Der-Chung Cheng Kanad Ghose

Department of Computer Science
State University of New York
Binghamton, NY 13902-6000
Email: ghose@bingvazu.cc.binghamton.edu
(607)-777-4608/(607)-777-4802

ABSTRACT

A barrier synchronizer, allowing processors to participate dynamically by letting them register their intent to participate within a timeout period, is presented. The synchronizer allows some applications - like software combining and highly concurrent queue operations - to be implemented in a rather unconventional but highly efficient manner. The barrier synchronizer generates successive time windows, allowing requests within the same window to be combined, thus ensuring a more-or-less fixed latency for the Fetch-and-Op primitive.