Proceedings of the 13th International Workshop on High-Level Programming Models and Supportive Environments

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This year marks the 13th instance of HIPS, the International Workshop on High-Level Programming Models and Supportive Environments. It is again held as a full day workshop in conjunction with the International Parallel and Distributing Processing Symposium (IPDPS), one of the premier events in the field of parallel processing. Since the workshop’s inception in 1996 it has established itself as a successful forum for researchers in the areas of computational models, language design, compilers, system architecture, and tools for large scale parallel systems.

We received many interesting and high-quality submissions and the program committee, after a careful and detailed review process, decided to accept seven of them. In addition, this year’s workshop includes two invited papers and keynotes by David Klepacki, IBM and Arch Robinson, Intel. We grouped these papers in three session focusing on tools in Session 1, on runtime mechanisms in Session 2, and on languages and compilers in Session 3.

Session 1 focuses on tools for high performance computing. It starts with an invited paper by David I-Hsin Chung, David Klepacki et al. describing an automatic approach to detect and analyze performance bottlenecks in high performance applications. The second paper in this session, by Isaac Dooley at al., examines noise in parallel applications and provides a toolset to identify and analyze such noise. In the third contribution in this session, Chee Wai Lee et al. discuss the use of data reduction techniques to enable a scalable analysis and visualization of performance data from highly parallel applications.

Session 2 discusses runtime systems and performance considerations for parallel environments. It is headed off with an invited paper by Arch Robinson et al. on optimized work stealing for the Intel Thread Building Blocks (TBB) and continues with a paper by Yoonju Lee Nelson et al. on the use modeling techniques to tune parameter values, which is demonstrated using a molecular dynamics application. The session is concluded with a paper by Farshad Khunjush et al. analyzing the DMA transfer characteristics on Cell processors.

Session 3 focuses on high-level parallel languages as well as compilers. The first paper in this session is by Aniruddha G. Shet et al. and discusses the programmability of the three new languages introduced as part of the HPCS efforts. Imran Patel et al. then describe an empirical study on the programmability of two radically different approaches to parallel programming based on their experiences in a programming class. The session is rounded off with a paper by Dibyendu Das et al. on static compiler optimizations to increase the computation/communication overlap by introducing and optimizing the use of non blocking communication primitives.

In addition to these three sessions, this year’s HIPS workshop also features a special session on the Performance Optimization of High-level Languages and Libraries (POHLL). This session was organized as a separate workshop by J. (Ram) Ramanujan from Louisiana State University and P. (Saday) Sadayappan form the Ohio State University. It features three papers, which were selected by a separate program committee. The large overlap in scope by HIPS and POHLL, however, makes this natural combination and we hope that our audience will profit from this additional interaction.

We would like to thank all authors who took the time to submit their papers to this year’s workshop as well as the program committee for their hard work and expertise in reviewing the papers. We also would like to thank the HIPS steering committee for their guidance and advice. We further extend our thanks to the organizing team of the International Parallel and Distributed Processing Symposium (IPDPS), our host conference, and in particular to Alan Sussman, the IPDPS workshop chair. All of them helped us to make this year’s workshop a successful event.

Martin Schulz and Sam Midkiff
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