Welcome to the second Workshop on Massively Parallel Processing. The workshop addresses all areas of massively parallel processing. In organizing this workshop, we recognize that computer solutions to many problems facing modern civilization require a level of computational power that far exceeds current capabilities. Consequently, we desired to solicit papers on research that extends current computational capacity boundaries and gives solutions to currently inaccessible computationally intensive problems, such as some of the grand challenge problems. General areas of interest include synchronous and asynchronous parallel computation, algorithms and models, systems architecture, hardware, systems software and languages, component technology, and applications. Specific topics of interest include SIMD and MIMD massively parallel systems case studies; teraflop and petaflop system development and applications; intelligent RAM, IRAM, and PIM system development; data parallel and associative computing; case studies and performance analysis of massively parallel systems and applications; resource management for massively parallel applications; domain specific libraries and applications; experience with commercial and experimental massively parallel systems; and systems software and tools for massively parallel computing. We hope that you will enjoy the selection of manuscripts that are contained in this conference program.
WORKSHOP ORGANIZERS

Workshop General Chair: Johnnie Baker

Program Chair: Philip A. Wilsey

Program Committee:

Nael Abu-Ghazaleh, SUNY Binghamton
Johnnie Baker, Kent State University
Hank Dietz, University of Kentucky
Ray Hoare, University of Pittsburgh
Mahmut Kandemir, Penn State University
Peter Kogge, Notre Dame University
Alice Koniges, LLNL
H. J. Siegel, Colorado State University
Theo Ungerer, University of Augsburg
Robert Walker, Kent State University
Philip A. Wilsey, University of Cincinnati

Publicity Committee: Nael Abu-Ghazaleh, Maher Atwah, and Ray Hoare

Webmaster: Robert Walker
Papers in the Workshop on Massively Parallel Processing

- “An SoC solution for Massive Parallel Processing,” D. Reed and R. Hoare

- “Modular Interconnection System for Optical PCB and Backplane Communication,” S. Age-lis, S. Jacobsson, M. Jonsson, A. Alping, and P. Ligander


- “Efficient Tiling for an ODE Discrete Integration Program: Redundant Tasks Instead of Trapezoidal Shaped-Tiles,” F. Rastello and T. Dauxois

- “Selecting Data Distributions for Unbounded Loops,” T. Tauber and G. Runger

- “The Case for Datacentric Grids,” D. B. Skillicorn

- “Load-Balanced Parallel Merge Sort on Distributed Memory Parallel Computers,” M. Jeon and D. Kim

