Surviving to Errors in Multi-Core Environments
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The continuous shrinkage of CMOS technologies and higher current densities make devices degrade much faster. The great challenge for future technologies is building reliable systems on top of unreliable components, which will degrade and even fail during the normal lifetime of the processor. Devising new approaches so that processors are resilient to lifetime degradation in a transparent manner for the users is crucial to reduce guardbands, and thus, achieve higher performance at lower power cost.

Multi-core is the new direction taken by the industry. Multi-cores enable linear scaling of performance for independent and parallelized programs within constrained power budgets.

Reliable and reconfigurable multi-core chips become mandatory to keep operating at full-throttle on the face of errors. Different mechanisms must be devised to:

1. Detect or anticipate errors so that data are not corrupted. Errors can be either anticipated by detecting components that will fail soon or detected immediately once they arise. Then, errors must be confined to the smallest possible component.
2. Estimate the degradation of the different components. Tracking the degradation of the different cores will be a key feature to activate error detection features in highly degraded cores and use non-degraded cores for critical tasks.
3. Reconfigure multi-cores to adapt to errors and degradation. Reconfiguring the multi-core involves setting up the proper operating parameters for each core, disable faulty ones and choose which cores must be used at any time.
4. Mitigate degradation. In order to provide higher performance during the whole lifetime of the processor it is mandatory mitigating degradation of the different cores due to electromigration, NBTI, TDDB, etc.

All those mechanisms must work coordinatey to increase the reliability of the processor without compromising its performance. Furthermore, that should be achieved at low cost.

We present a global view of the issues outlined above as well as some directions to address them. First, the most important sources of failure (SOF) are presented as well as their impact on CMOS technology. Then, techniques and key parameters to measure degradation due to different SOF are introduced and microarchitectural approaches to mitigate degradation are outlined. The problem of error detection and anticipation is illustrated as well as pros and cons of different types of mechanisms to perform such detection and anticipation. Finally, we illustrate the whole picture where performance and reliability must be traded carefully. We point out some directions to use the information about the detected errors and the amount of degradation of each component to configure the multi-core in such a way that performance is maximized without compromising reliability.