GRAAL: A Fault-Tolerant Architecture for Enabling Nanometric Technologies

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Silicon-based CMOS technologies are fast approaching their ultimate limits. By approaching these limits, power dissipation, fabrication yield, and reliability worsen steadily making further nanometric scaling increasingly difficult. These problems would stop further scaling of silicon-based CMOS technologies at channel lengths between 10 and 20 nm. But even before reaching this level of integration, these problems could become show-stoppers unless new techniques are introduced to maintain acceptable levels of power dissipation, yield and reliability. The paper describes the principles of GRAAL (Global Reliability Architecture Approach for Logic), a new fault tolerant architecture for logic designs. This architecture is aimed to provide a global solution for mitigating the flaws of deep nanometric technologies related to power dissipation, yield and reliability.