Heavy Ion Test Results in a CMOS triple Voting Register for a High-Energy Physics Experiment

X. Cano¹, S. Bota², R. Graciani³, D. Gascón³, A. Herms¹, A. Comerma³, J. Segura², L. Garrido³
¹ Dept. Electrònica, U. Barcelona. ² GTE, U. Illes Balears. ³ Dept. ECM, U. Barcelona. Spain
xcano@ub.edu

Abstract

A heavy ion radiation test has been performed to evaluate the SEU sensitivity on a mixed-mode ASIC. We present the results obtained when the Triple Voting Registers used in the digital block of the ASIC are irradiated with heavy ions.

1. Introduction

LHCb [1] is a dedicated experiment to study B-meson physics at CERN. We have designed an ASIC dedicated to discriminate the signals supplied by a 64-anode photomultiplier in response of particle hits resulting from particle collisions. These collisions produce a radiation environment that can damage the apparatus. For single event effects it is important to ensure that the time between failures is sufficiently long to guarantee an effective running of the whole experiment over extended periods or over the life experiment.

2. ASIC design

The photomultiplier signal is amplified, shaped and discriminated through a mixed-mode ASIC [2]. A BiCMOS 0.8µm technology was chosen in order to take benefit from the advantages of bipolar transistors for high transconductance and low offset stages of CMOS transistors for the digital block and analogue switches. Each ASIC processes eight different sub-channels of a 64-channel photomultiplier. To be able to compensate the offsets due to process variations between different sub-channels, two different threshold values for each sub channel are stored in digital registers.

Each register is a two-level register (Fig. 1). Configuration data is stored at EFF registers. DFF flip-flops have been connected in series, forming a Scan-path used to write/read the data stored at EFF registers.

During the ASIC design phase some techniques were applied to improve radiation tolerance. For example, the digital block used to program the threshold values was designed full-custom, guard rings were introduced to prevent latch-up and to protect against noise and cumulative effects, we use NAND gates wherever possible instead of NOR gates to be less sensitive to accumulative effects. Each register (both, EFF and DFF) is formed by a master and three slaves connected in parallel to perform triple voting (TVR). The master is updated every clock cycle (positive edge) using the value computed by a majority block that use the logic state of the three slaves as inputs. So, two of the slave latches must be affected by a single event effect to produce an error. Although the error probability for unit area is constant, this decrease with the duty cycle, because when the master is latched it is sensitive to SEU.

![Figure 1. Detail of 1bit register](image)

3. Experiment

The digital block of the ASIC consists of two 14 bit-registers per channel. These are loaded from an independent serial shift-register and Control Unit that allow implementing the read, write and load operations over the internal registers protected by the TVR. A Krypton beam with an energy of 73 MeV/A has been used to irradiate the chips. Introducing different layers of Aluminum as absorber up to 900 mm, gives LET(dE/dx) values in the range of 9.55-15.21 MeVcm²/mg.
The test included several ASICs read-back in daisy chain configuration, which allowed synchronous access to a total of 56 bits. To determine the error cross section the following expression has been used:

\[ \sigma = \frac{N_{\text{events}}}{\phi N_{\text{bits}}} \text{ cm}^2 / \text{bit} \]

Where \( N_{\text{events}} \) is the number of errors, \( N_{\text{bits}} \) is the number of bits (56) and \( \phi \) is the fluence, total number of ions by unit of area.

The measured cross-section is plotted in Fig. 2, where a fitted Weibull approximation is also shown. With the cumulated probability distribution the main characteristic parameters by channel (14 bits) are:

- LET threshold = 9±0.5 MeV·cm²/mg
- SEU cross-section = 1.1±0.1 \( 10^{-6} \) cm²/ch.

To study the effect of the triple voting the set-up was modified to change the duty cycle from 1% to 99%. The data is shown in Fig. 3 over the initial results that were obtained with a duty cycle of 50%. The little improvement observed when the SEU cross-section is multiplied by a factor 7 is less than expected. That let some open questions about the internal behavior and the effectiveness of the TVR system.

The SEU contribution from the shift registers would manifest itself into a slope in the observed error rate as function of the position of the register. Since the last register of the chain remains 56 times longer than the first one. The measured slope is compatible with zero, thus this contribution is neglected. Nevertheless, a clear asymmetry is observed between bits set to 1 and those set to 0. Both effects can be observed in Fig. 3. Usually, the out-of-the-well off-transistor drain is more sensitive to SEU than other device regions [3]. This means that in our latch design, the probability to induce an upset is higher when the nMOS transistor of the input inverter of the non-redundant master latch is in their off-state (master internal node initially set to 1). Taking into account that the master latch is storing the complementary state of the register, this implies that the number of 0-to-1 transitions due to SEU observed in the register output, will be greater than 1-to-0 transitions. SEU effects occurred at the transistors of slave registers will be corrected by TVR.

4. Discussion

The poor improvement in the SEU ratio as a function of the clock duty cycle of the Triple Voting Operation, leads to a deeper analysis.

5. References