Managing Large Health Care Data

by

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Wireless Sensor Networks (WSNs) were primarily introduced for defense application, with an objective of monitoring enemy’s activities without any human intervention. In recent years, introduction of IoT has added another dimension to volume of data. In this talk, we consider two complimentary scheme of handling data for instantaneous sensing and 24x7 transmitting important physiological signals. The first step consists of transmitting biomedical data at needed rate without affecting accuracy of results. The second step involves aggregation of data over period of time. Pulmonary Artery Pressure (PAP) and Electrocardiogram (ECG/EKG) are selected as two preliminary physiological signals for Cardio-Vascular Diseases (CVDs). We use a Wireless Body Area Sensor Network (WBASN) to get the physiological data from a user’s body and transmit them to a WBAN coordinator. The second step is to aggregate sensor data by combining overtime as signals change slowly over time. Effectiveness of such an aggregation scheme is illustrated by measuring the degree of compression for EEG scalp readings, gait measurement in patients with neurodegenerative conditions, and motor movement signals in normal subjects. Final comments are added to provide glimpse of what can be done to handle volume of biomedical data in the context of IoT.

Short Biography of Dharma P. Agrawal

Dharma P. Agrawal is the Ohio Board of Regents Distinguished Professor and the founding director for the Center for Distributed and Mobile Computing in the Department of Electrical Engineering and Computing Systems. He has been a faculty member at the ECE Dept., Carnegie Mellon University (on sabbatical leave), N.C. State University, Raleigh and the Wayne State University. His current research interests include applications of sensor networks in monitoring Parkinson’s disease patients and neurosis, applications of sensor networks in monitoring fitness of athletes’ personnel wellness, applications of sensor networks in monitoring firefighters physical condition in action, efficient secured communication in Sensor networks, secured group communication in Vehicular Networks, use of Femto cells in LTE technology and interference issues, heterogeneous wireless networks, and resource allocation and security in mesh networks for 4G technology. His recent contribution in the form of a co-authored introductory text book on Introduction to Wireless and Mobile Computing, 4th edition has been widely accepted throughout the world and fourth edition is in press. The book has been has been reprinted both in China and India and translated in to Korean and Chinese languages. His co-authored book on Ad hoc and Sensor Networks, 2nd edition, has been published in spring of 2011. A co-edited book entitled, Encyclopedia on Ad Hoc and Ubiquitous Computing, has been published by the World Scientific and co-authored books entitled Wireless Sensor Networks: Deployment Alternatives and Analytical Modeling, and Innovative Approaches to Spectrum Selection, Sensing, On-Demand Medium Access in Heterogeneous Multihop Networks, and Sharing in Cognitive Radio Networks have being published by Lambert Academic. He is a founding Editorial Board Member, International Journal on Distributed Sensor Networks, International Journal of Ad Hoc and Ubiquitous Computing (IJAHUC), International Journal of Ad Hoc & Sensor Wireless Networks and the Journal of Information Assurance and Security (JIAS). He has served as an editor of the IEEE Computer magazine, and the IEEE Transactions on Computers, the Journal of Parallel and Distributed Systems and the International Journal of High Speed Computing. He has been the Program Chair and General Chair for numerous international conferences and meetings. He has received numerous certificates from the IEEE Computer Society. He was awarded a Third Millennium Medal, by the IEEE for his outstanding contributions. He has delivered keynote speech at 38 different international conferences. He has published over 666 papers, given 57 different tutorials and extensive training courses in various conferences in USA, and numerous institutions in Taiwan, Korea, Jordan, UAE, Malaysia, and India in the areas of Ad hoc and Sensor Networks and Mesh Networks, including security issues. He has graduated 70 PhDs and 58 MS students. He has been named as an ISI Highly Cited Researcher, is a Fellow of the IEEE, the ACM, the AAAS and the World Innovation Foundation, and a recent recipient of 2008 IEEE CS Harry Goode Award. Recently, in June 2011, he was selected as the best Mentor for Doctoral Students at the University of Cincinnati. Recently, he has been inducted as a charter fellow of the National Academy of Inventors. He has also been elected a Fellow of the IACSIT (International Association of Computer Science and Information Technology), 2013.
Spot Defect Modeling: History and Perspectives

by

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Abstract:

With today manufacturing technology, it is not possible to eliminate all defects and ensure every manufactured unit is perfect. Instead, each manufactured unit must be tested so that defective parts are not shipped to a customer. Different Test Strategies are commonly used since none is considered as optimal in terms of low defect level. Most companies use some but not all of the following three Test Strategies: the Static Voltage strategy, the Dynamic Voltage or Delay strategy, the Static or Dynamic Current (I_{DDX}) strategy.

While using different approaches, these different test strategies have a common objective: reveal the presence in the chip of defects or deviations that may create a dysfunction. Knowing the complexity of today defects, it is admitted that the classical fault models used for test generation cannot guarantee a satisfactory detection of defects. This implies that new test generation technique specifically oriented to defects have to be defined. So, we must analyze and understand the electrical behavior of the defect and describe its behavior through an adequate ‘defect model’. Then, defect simulation techniques and defect-oriented ATPG techniques must be proposed to allow specific test generation for these defects.

This presentation focuses on spot defects that manifest themselves as shorts or opens in the interconnect or in the MOS transistors: ‘Interconnect open’, ‘Interconnect short’, ‘Floating gate’, and ‘Gate-Oxide-Short’ are analyzed in detail using different model levels. For every defect, it is shown that the electrical behavior is in fact not predictable due to the presence of random parameters. In order to tackle the problem of unpredictability, unified concepts are proposed that allow new test generation techniques guaranteeing coverage of unpredictable defects.

Short Biography:

Michel Renovell joined in 1986 the Laboratory of Computer Science, Robotics and Microelectronics of Montpellier (LIRMM) where he was a researcher funded by the French National Council for Scientific Research (CNRS). From 1995 to 2005, he served as head of the Microelectronics team and he is now Deputy-Director of LIRMM (420 staff members). Since 2006, he also serves as Assistant-Director for the CNRS National Institute for Information Sciences (INS2I) managing more than 60 labs in France. He is a member of the editorial board of JETTA and the VLSI Journal. Michel was member of the editorial board of IEEE Design & Test general and he was chair or program chair of many conferences (ETS, VTS, DELTA, IMSTW, FPL, SBCCI, DDECs...). He has published over 240 international papers and has received several best paper awards. In 2013 he has been nominated ‘IEEE Fellow’ for his contribution to ‘Defect Modelling’. His research interests include: Defect modelling, Analog testing and FPGA testing.
The Automata Processor (AP) developed by Micron Semiconductor is a fundamentally new hardware computing architecture capable of performing high-speed, comprehensive search and analysis of complex, unstructured data streams. A highly scalable fabric of interconnected processing elements, the AP delivers unprecedented, energy efficient parallelism while avoiding many of the complexities inherent in standard parallel programming. The Automata Processor is especially powerful because it implements natively in hardware the non-deterministic finite automata (NFA) paradigm from classic computer science theory. The non-determinism property allows many states to be active at once. This allows the AP to explore many potential candidate matches in parallel, thus making it capable of solving "fuzzy" matching problems, even those with combinatorial search spaces. In this regard, it bears some similarity to quantum computing. The AP is particularly effective at leveraging this property thanks to its large capacity. A single chip holds over 49,000 states, all of which are concurrently scanning and responding to the input stream; and Micron's initial boards will hold 32 chips, thus providing over 1.5 million states, all operating concurrently. The speaker is co-director of the UVA Center for Automata Processing (CAP) co-founded by Micron Semiconductor and the University of Virginia for fostering fundamental research on foundations and applications of automata computing.

http://cap.virginia.edu/

http://www.micronautomata.com/
Short bio

Mircea R. Stan received the Ph.D. (1996) and the M.S. (1994) degrees in Electrical and Computer Engineering from the University of Massachusetts at Amherst and the Diploma (1984) in Electronics and Communications from "Politehnica" University in Bucharest, Romania. Since 1996 he has been with the Charles L. Brown Department of Electrical and Computer Engineering at the University of Virginia, where he is now a professor. Prof. Stan is teaching and doing research in the areas of high-performance low-power VLSI, temperature-aware circuits and architecture, embedded systems, spintronics, and nanoelectronics. He leads the High-Performance Low-Power (HPLP) lab and is a co-director of the Center for Automata Processing (CAP). He has more than eight years of industrial experience, has been a visiting faculty at UC Berkeley in 2004-2005, at IBM in 2000, and at Intel in 2002 and 1999. He has received the NSF CAREER award in 1997 and was a co-author on best paper awards at ISQED 2008, GLSVLSI 2006, ISCA 2003 and SHAMAN 2002. He was the chair of the VLSI Systems and Applications Technical Committee (VSA-TC) of IEEE CAS in 2005-2007, general chair for ISLPED 2006 and for GLSVLSI 2004, technical program chair for NanoNets 2007 and ISLPED 2005, and on technical committees for numerous conferences. He is a Senior Editor for the IEEE Transactions on Nanotechnology since 2014, and was an AE for the IEEE Transactions on Nanotechnology in 2012-2014, IEEE Transactions on Circuits and Systems Systems I in 2004-2008 and for the IEEE Transactions on VLSI Systems in 2001-2003. He has also been a Guest Editor for the Computer special issue on Power-Aware Computing in December 2003 and a Distinguished Lecturer for the IEEE Circuits and Systems (CAS) Society in 2012-2013 and 2004-2005, and for the Solid-State Circuits Society (SSCS) in 2007-2008. Prof. Stan is a fellow of the IEEE, a member of ACM, and also ofEta Kappa Nu, Phi Kappa Phi and Sigma Xi. His current h-index is 43 and i10-index is 101.
Improving Yield and Reliability of Chip Multiprocessors in Nanotechnology

Sandip Kundu

Abstract

Device reliability and manufacturability have emerged as dominant concerns in end-of-road CMOS and emerging nanotechnology devices. An increasing number of hardware failures are attributed to manufacturability or reliability problems. ITRS vision been described as:

“Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test. Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.”

Maintaining an acceptable manufacturing yield for chips containing tens of billions of transistors with wide variations in device parameters has been identified as a great challenge. Additionally today's nanoscale devices suffer from accelerated aging effects because of the extreme operating temperature and electric fields they are subjected to. Unless addressed in design, aging-related defects can significantly reduce lifetime of a product.

In this talk, we will discuss microarchitectural techniques for improving yield and reliability of homogeneous chip multiprocessors (CMP). The key concepts involve a hardware framework to enables utilizing the redundancies inherent in a multi-core system to keep the system operational in face of partial failures. We engage the existing resources to implement spatial and temporal redundancy. Such a service improves yield and reliability, at a slight loss of performance.

We will present results to show the feasibility and practicality of the solutions.

Biography

Sandip Kundu is a Professor at the University of Massachusetts at Amherst. Prior to joining academia, he spent several years in industry: first as a Research Staff Member at IBM Research Division and then at Intel Corporation as a Principal Engineer. He has published over 200 research papers in VLSI design and test and holds several key patents including ultra-drowsy sleep mode in processors, and has given more than a dozen tutorials at various conferences. He is a Fellow of the IEEE, Fellow of the Japan Society for Promotion of Science (JSPS) and a Distinguished Visitor of the IEEE Computer Society. He is currently an Associate Editor of the ACM Transactions on Design Automation of Electronic Systems. Previously, he has served as an