Tutorial T4B
Design Challenges for High Performance Nano-Technology

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Abstract
This tutorial presents the key aspects of design challenges and their solutions that are being experienced in VLSI design in the era of nano technology. The focus will be on design challenges that are experienced in microprocessor designs. It will capture the design issues in the areas of high level architectural modeling, design for manufacturability (DFM), layout synthesis, standard cell design, and performance verification. It will describe the requirements to meet power, timing, physical dimension and process portability goals with nano-technology. It will also address the pre and post silicon verification difficulties that have a direct impact on taking the product to market.

This tutorial covers the following main topics in detail:

- Expectation from the VLSI product (Moore’s law, Higher performance, higher clock speed, smaller die, lower dynamic and static power, higher reliability)
- High level Modeling Challenges that includes power modeling, performance analysis, DFT and HVM modeling and RTL estimation of key design metrics.
- Design-for-Manufacturability (DFM) challenges; Nano process physical design, extraction, reliability.
- Design-for-Test challenges that addresses DFT strategy and planning, Fault models, Full/partial scan design, and special test structures.
- Performance verification that describes the limitation of static timing model, affect of small devices, higher temperature impact from a dense area, voltage drop due to on die variation, etc.
- Standard cell library usage and design is critical to achieve higher Fmax. It will address standard cell layout architecture, granularity of library strength, parameterized cells.
- Layout synthesis using congestion minimization process, intelligent partitioning and clock tree synthesis for high density design.
- Post silicon debugging and process correlation; Special circuit verification, power budget verification, process correlation issues, DPM prediction, reliability verification and Burn-in

Presenter Biography

Goutam Debnath received a B.S (Hons) degree in Physics from Scottish Church College, Calcutta, India. He received a M.S (Thesis) in Physics from University of St Louis, Missouri, USA and a M.S. (Thesis) in Electrical Engineering from Southern Illinois University, Carbondale, USA. Goutam is presently a Design Automation and Convergence manager for microprocessor designs at Intel Corporation. He has done 14 Intel based desktop processors and 4 Xeon processor in last 14 years of Intel’s professional carrier. His primary interest and focus is to improve the design methodology to handle current design challenges for the deep submicron technology and improve the reliability and the quality of the design. Goutam has published and co-authored 8 technical papers in numerous conference including IEEE and VLSI conference. He has two USA patents on clock distribution in control logic blocks and shared power grid distribution respectively.

Paul Thadikaran received his Ph.D. in Computer Science from State University of New-York, Buffalo. He is currently a Principal Engineer at the Enterprise Microprocessor Development Group at Intel Corporation. He is also an Adjunct Professor at the Oregon Health Sciences and Engineering University (OHSU). He has been involved in various aspects of design and test of previous three generations of Intel’s IA-32 CPU. He has managed CAD tool development and standard cell library development targeted for CPU designs for past six years. His areas of interest
include CAD tools and algorithms for test generation, power estimation, verification and diagnosis. Paul has published more than 15 papers in IEEE/Intel conferences and journals. He has also co-authored a book on \( I_{ddq} \) Testing published by Kluwer Academic Press. Paul has refereed several IEEE and ACM journals such as IEEE Transactions on CAD, ACM Transactions on design automation in electronic systems (TODAES).

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