Abstract
This tutorial focuses on advanced techniques to cope with the complexity of designing modern digital chips which are complete systems often containing multiple processors, complex IP blocks and high-speed buses and interconnection networks. This tutorial addresses the following emerging challenges: architectural exploration, HW/SW co-design, complex control and concurrency, correctness and verification, timing closure, and low-power.

The tutorial will focus on language facilities and synthesis techniques that dramatically simplify and shorten the process of correct chip design by raising the level of abstraction on multiple dimensions without sacrificing final hardware quality. The tutorial will cover the following topics in detail:

High-Level Language Facilities:
- Modeling concurrency and managing shared resources with atomic rules
- Building scalable designs with modules and rule-based interfaces
- Synthesizing rules into hardware, including scheduling
- Improving correctness through advanced types and type-checking
- Managing power with systematic clock domains
- Leveraging advanced parameterization to promote reuse

Methodologies:
- Systematic refinement from transaction-level models to synthesizable implementations
- Architectural exploration for optimal designs
- Simulation and co-simulation of complex systems
- How verification is shortened by designing with abstraction
- Systematic debugging/verification: functional correctness vs. performance correctness
- Systematic modification for timing closure: retiming and rebalancing

Lectures will include numerous code examples and walk-throughs

Presenter Biography

Rishiyur S. Nikhil, Ph.D. (Nikhil) has spent over 20 years in advanced technical pursuits in industry and academia. Having led the Bluespec technology team from 2000-2003 at Sandburst, Inc., since then he has been CTO and co-founder of Bluespec, Inc. He was at Cambridge Research Laboratory (DEC/Compaq) from 1991-2000, including over a year as Acting Director. Earlier, he was an Associate Professor of Computer Science and Engineering at MIT. He has led research teams, published widely, and holds several patents in functional programming, dataflow and multithreaded architectures, parallel processing and compiling. He is a member of ACM, IEEE, and IFIP WG 2.8 on Functional Programming. He received his Ph.D. and M.S.E.E. in Computer and Information Sciences from the Univ. of Pennsylvania, and his B.Tech in EE from IIT Kanpur.

Shiv Tasker (Shiv) is a co-founder and the CEO of Bluespec, Inc.. Prior to Bluespec, Shiv was the president and CEO of Phase Forward, a software and service solution vendor for the data collection and management of clinical trials of new drugs and devices. Prior to Phase Forward, Shiv was Sr. Vice President for Worldwide Sales, Consulting Services and Corporate Marketing at Viewlogic Systems Inc, a supplier of complex electronic design automation tools for Integrated Circuit and Printed Circuit Board design. Previously, Mr. Tasker spent eight years at...
Cadence Design Systems in a variety of roles in marketing and general management and was with Intergraph Corp for almost six years, initially as an engineer and later as a marketer. Mr. Tasker holds an MBA from the University of Texas at Arlington and a BS from the University of Bombay in Statistics and Economics.

**Contact Information**

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