Abstract

This tutorial discusses design challenges of scaled CMOS circuits in sub-90nm technologies and the design methodologies required to design them in order to produce robust designs with desired power performance trade-off. It is increasingly difficult to sustain supply and threshold voltage scaling to provide the required performance increase, limit energy consumption, control power dissipation, and maintain reliability. These requirements pose several difficulties across a range of disciplines. On the technology front, the question arises whether we can continue along the traditional CMOS scaling path – reduce effective oxide thickness, improve channel mobility, and minimize parasitics. On the design front, researchers are exploring various circuit design techniques to deal with process variation, leakage and soft errors. We will focus on the following components:

Design challenges of sub-90nm CMOS circuits with particular emphasis on implications of each individual device scaling element on circuit design: To continue scaling of the CMOS devices deep into sub-90nm technologies, fully depleted SOI, strained-Si on SiGe, FinFETs with double gate, and even further, three-dimensional circuits will be utilized to design high-performance circuits. We will discuss unique design aspects and issues resulting from this scaling such as gate-to-body tunneling, self-heating, reliability issues, and process variations. As the scaling approaches various physical limits, new design issues such as $V_t$ modulation due to leakage, low-voltage impact ionization, and higher $V_{tun}$ to maintain adequate $V_{t, sat}$ continue to surface. In this part of tutorial, we will discuss these emerging trends and design issues related to aggressive device scaling.

Managing leakage power: It is well known that with CMOS technologies beyond 90nm, leakage power is one of the most crucial design components which must be efficiently controlled in order to utilize the performance advantage from these technologies. We will focus on various techniques to analyze and control all components of leakage power placing particular emphasis on sub-threshold and gate leakage power. In addition, this part of tutorial will discuss low voltage circuit design under high intrinsic leakage, leakage monitoring and control techniques, effective transistor stacking, multi-threshold CMOS, dynamic threshold CMOS, well biasing techniques, and design of low leakage data-paths and caches.

Circuit Design in the Presence of Uncertainty: Nanometer design technologies must work under tight operating margins, and are therefore highly susceptible to any process and environmental variabilities. This part of the tutorial will consider several factors related to reliability and yield. With regard to environmental variations, it is important to build circuits that have well-distributed thermal properties, and to carefully design supply networks to provide reliable $V_{dd}$ and ground levels throughout the chip. On the process variation front, the effects of uncertainties in process variables must be modeled using statistical techniques, and they must be utilized to determine variations in the performance parameters of a circuit. Instead of pessimistically treating timing in a worst-case manner as is conventionally done in static timing analysis, statistical techniques will have to be employed that directly predict the percentage of circuits that are likely to meet a timing specification.

Parameter Variation Tolerance: We will cover the components of variation and some circuit techniques to address variation tolerance. Process variation has also received increased attention from design automation community. Traditional sources of variation due to circuit and environmental factors also affect circuit performance significantly. These are cross capacitance, power supply integrity, multiple input switching, errors arising due to tools and flows, etc. We will present these sources and quantify their impact on high-speed microprocessor performance.

Radiation-induced single event upsets (SEUs): Soft errors pose a major challenge for the design of memories and logic circuits in high-performance microprocessors in technologies beyond 90nm. Soft errors and single event upsets are gaining increased attention as the technology scales. Measured data shows 8% soft error rate (SER) increase per...
bit per technology generation. As the number of memory bits and sequential elements increases across generations, the soft error problem is likely to become a serious barrier for advanced microprocessors. Historically, we have considered power-performance-area tradeoffs. There is a need to include the SER as another design parameter. In this tutorial, we also present radiation particle interactions with silicon, charge collection effects, soft errors, and their effect on VLSI circuits. We also discuss the impact of SEUs on system reliability. We describe an accelerated measurement of SER using a high-intensity neutron beam, the characterization of SER in sequential logic cells, and technology scaling trends. Circuit techniques for soft error tolerance are also presented with their relative benefit.

**Presenter Biography**

**Ruchir Puri** is a Research Staff Member in Design Automation and VLSI Design group at IBM T J Watson Research Center since 1995. He received M.Tech. degree in electrical engineering from Indian Institute of Technology, Kanpur, India in 1990, and a Ph.D. degree in computer engineering from University of Alberta, Canada in 1994 where he received ACM/IEEE design automation scholarship for his research. His current research interests include logic, physical design issues for IBM's low-power and high-performance microprocessors and ASICs. He has also been responsible for analyzing and evaluating the design and reliability issues involved in implementing high-performance circuits in advanced technologies. He is inventor of 12 issued/pending U.S. patents and has authored over 50 papers including chapters in John Wiley’s Encyclopedia of Electrical & Electronics Engineering and Encyclopedia of Computer Science. His paper on domino logic synthesis was rated the best synthesis paper in ICCAD-96 and the patent related to this research also received IBM's significant patents award. He was an adjunct assistant professor in Electrical Engineering at Columbia University, New York where he taught VLSI design and Circuits during 2000-01. He has served on technical program committees of several conferences and National Science Foundation review panels. He has also presented/authored tutorials at various conferences such as ICCAD, VLSI Design, ISSCC. He is included in Marquis “Who's Who in America” and "Who's Who in Science and Engineering”.

**Tanay Karnik** (M’88, SM’04) is a Principal Engineer at Circuit Research Lab in Intel. He received his Ph.D. in Computer Engineering from the University of Illinois at Urbana-Champaign in 1995. From 1995 to 1999, he worked in the Strategic CAD Lab at Intel working on RTL partitioning, physical design and special circuits layout. Since March 1999, he has lead the power delivery, soft error rate, and optoelectronic circuits research in the Circuits Research, Intel Labs. Earlier, from 1987 to 1988, Tanay worked on programmable logic controller design at Larsen & Toubro Ltd.* in India. He spent the summer of 1994 at AT&T Bell Labs* developing a timing and synthesis module for FPGAs. His research interests are in the areas of power delivery, soft errors, voltage regulator module (VRM) circuits, leakage tolerance and physical design. He has published over 30 technical papers, has 17 issued and 47 pending patents in these areas. He has presented several invited talks and tutorials. He serves on ICCAD, ISQED, DAC and ICICDT committees. He is on the review committees of JSSC, TCAD, TCAS and TVLSI. He will serve as the TPC Chair for ISQED’06. He has also graduated 3 PhD students as an industrial advisor.

**Rajiv V. Joshi** is a research staff member at T. J. Watson research center, IBM. He received his B.Tech degree from Indian Institute of Technology (Bombay, India), M.S degree from Massachusetts Institute of Technology and Doctorate in Eng. Science from Columbia University, USA. From 1981 to 1983, he was with GTE research lab in Waltham, Massachusetts. He joined IBM in Nov. 1983, and since then is working in VLSI design systems, science and technology. He worked on 1.25um NMOS, and CMOS, sub-0.5um CMOS logic, DRAM and SRAM technologies. His work involves development of novel interconnect processes and structures for Aluminum, tungsten and Copper technologies which are widely used in IBM for various sub-0.5um memory and logic technologies as well as across the globe. His circuit related work includes design of register files, registers, latches, L1 caches, Directory, TLB, IO circuits development of physical design tools, and CAD based library generation and circuit designs in SOI technology. He contributed to S/390 Alliance processor design, working in both circuit design and CAD tools. The Alliance G5 chip was a very successful IBM product and Joshi received IBM Research Division Awards for his contributions to it and each of the follow-on processor designs. His 2 GHz SRAM design for G6 received Outstanding technical achievement award. His work also involved design related to SRAM which are widely used across IBM System 390. He has won twenty-six invention plateau achievement awards from IBM and won two patent portfolio awards for cross-licensing and utilization of his patents in the IBM products. He has received 5 Research Division Awards, and several top 5% patent awards (for licensing activities). He received two Corporate Patent Portfolio award from IBM. He is a master inventor & key technical leader at IBM research.
division. He has authored and co-authored over 100 research papers and presented several invited and keynote talks. He holds 80 U.S. patents in addition to 40 pending patents. He received the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference. He was instrumental in starting interconnect workshop in early 1980s. He chaired advanced interconnect conferences sponsored by MRS and served as an editor of the proceedings.

He was elected as an IEEE fellow in 2002 for contributions to chip metallurgy materials and processes, and high performance processor and circuit design. He is actively involved in IEEE ISLPED, IEEE VLSI design, IEEE Int. SOI conf Program committees.