Energy-Aware Compiler scheduling for VLIW Embedded Software

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Abstract

In most of compilers, the goal of traditional instruction scheduling algorithms is to improve performance in terms of execution time. This can be done by some well-known ways such as superblock scheduling, hyperblock scheduling, and treegion scheduling. These scheduling strategies focus mainly on increasing performance through increasing the amount of instruction-level parallelism in program code. However, in VLIW (very long instruction word) architectures, an instruction word consists of a variable number of individual instructions. Therefore the step power and peak power consumption vary significantly depending on the parallel schedule generated by compiler. Power variation reduction without losing execution speed is an important scheduling constraint for embedded VLIW architectures. In this talk, we will introduce some power-aware scheduling strategies for VLIW processors. These scheduling methods include

- low power scheduling for basic blocks with integer programming
- Modulo and Software Pipelining for loops
- Register allocation and cache reuse for power reduction.

With these techniques, switch activities between instructions can be minimized so that power consumption can be reduced significantly.

References


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