Panel Discussion: How Much Longer Will SuperScalar Microarchitectures Scale?

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Abstract

According to many recent limit studies, most applications have enormous quantities of unharvested instruction-level parallelism. Despite great efforts, however, current high-end processors still only sustain about one instruction per cycle, on a good day. Once clock rate improvements start to slow substantially, the bulk of the performance growth will have to come from ILP. This panel, composed of renowned architects from industry and academia, will debate whether evolutionary superscalar architectures will be up to the task, or whether they must be replaced due to power, complexity, cost, or fundamental performance limitations.