The Power4 processor is a greater than 1.3GHz clock frequency, 174 million transistor chip, containing 2 microprocessor cores, high speed busses and an on-chip memory sub-system. The complexity, high frequency and size of the Power4 presented a number of significant challenges for its multi-site design team. The design of the Power 4 microprocessor required an innovative design methodology combining both IBM internally developed software with vendor tools. The challenge was to complete the design of a complex microprocessor on schedule and to specification. This required exploiting the hierarchical nature of the design and enabling parallelism of effort across three distinct phases of design (High Level Design, Schematic Design, Physical Design). New circuit tuning tools and methodologies were implemented to improve circuit speed and design productivity. Tools and methodologies had to be significantly improved for chip integration to manage, power, noise, long wires, timing, checking, etc. on a huge chip.