Clear and Present Tensions in Microprocessor Design

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Abstract

Microprocessor performance can be improved by increasing either the clock frequency (GHz) or the instruction level parallelism (IPC) or both. There is a complex and adversarial relationship between increasing GHz and increasing IPC. This talk revisits the old “speed-demons vs. brainiacs” debate (in some sense the reincarnation of the “RISC vs. CISC” debate) and recasts it as the tension between performance and implementation efficiency. Hardware and software evolve at widely differing rates. Hardware designs evolve quickly to take advantage of each new technology generation. Legacy software tends to persist for decades. There is also a strong trend towards portable code. There is an increasing incompatibility between legacy/portable code and the latest/best execution cores. To achieve performance and efficiency, future microprocessor designs must effectively manage this tension between hardware and software

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