A GaAs Receiver Module for Optoelectronic Computing and Interconnection

Joongho Choi, Bing J. Sheu

Department of Electrical Engineering
and National Center for Integrated Photonic Technology
University of Southern California
Los Angeles, CA 90089-0271

ABSTRACT
A GaAs gigahertz optical receiver module is designed and fabricated through an MESFET technology. This receiver and the associated laser diode based transmitter are suitable for integrated optoelectronic signal processing and optical neurocomputing.

I. Introduction
As optical computing becomes more popular, integrated optical receivers and laser diodes are in great demand. Due to the monolithic integration of arrays of optical receivers, optical neurocomputing can be implemented in compact hardware. One application example of optical computing is shown in Fig. 1, in which the electrical switching module consists of an array of optical receivers and laser diodes.

Optical receivers, which require a very large gain-bandwidth product for high sensitivity, were fabricated by bipolar silicon technologies or fine-line CMOS technologies. However, for the operation speed of more than 1 GHz, advanced fabrication technologies based on compound semiconductors such as InP, InGaAs, and GaAs, are needed. As the GaAs MESFET technologies become more mature, various analog circuits can be integrated into the chip, which makes the single-chip optical data interface possible. This data interface includes the optical receiver with the pre-processor and the post-processing elements for the next stage of signal processing. Integrating the optical data interface into the chip with digital circuitry makes an optical data processing system on a single chip achievable.

In this paper, an optical receiver operating at over 1 GHz is designed for the general-purpose optical data interface using a GaAs technology. Design techniques are employed to increase the bandwidth of the receiver circuit. In addition, basic digital circuits are also fabricated to extract technology parameters and to provide information for higher levels of integration.

II. Design of a Transimpedance Optical Receiver
There are two main types of optical receivers: the high impedance amplifier and the transimpedance amplifier [1]. In the high impedance amplifier, the input equivalent noise current is very low due to the high input resistance. However, the dynamic range is limited because of saturation of the amplifier output. In addition, it needs an equalizer for pole-zero cancellation after the optical signal is converted into a voltage. This is difficult to implement since the exact value of the capacitance is hard to control, especially for the receiver array, in a GaAs technology. In the transimpedance amplifier, the equalizer is not required and there is no major limiting mechanism of the dynamic range. However, in terms of the feedback resistance, high sensitivity and large bandwidth cannot be achieved simultaneously. Increasing the feedback resistance, \( R_f \), increases the sensitivity of the input photo-current, but decreases the bandwidth.

The detailed circuit schematic of the transimpedance amplifier configuration that is chosen as the optical receiver is shown in Fig. 2. Depletion-mode MESFETs with a minimum gate length of 1.2 \( \mu \text{m} \) are used. A simple, planar metal-semiconductor-metal photodiode is used to reduce the input capacitance of the amplifier [2]. An inter-finger gate metal is used for this MSM photodiode, with finger width of 1.2 \( \mu \text{m} \) and spacing between fingers of 1.6 \( \mu \text{m} \). The estimated capacitance of a 20 \( \mu \text{m}^2 \) photodiode is around 0.1 pF. This low capacitance can improve the bandwidth and noise performance. The feedback resistance is implemented by a transistor biased in the triode region in order to reduce the associated parasitic capacitance. If the passive resistor is used, a large area is needed for the large resistance value that ensures a high sensitivity and transimpedance gain. The parasitic capacitance associated with this passive resistor will degrade the bandwidth and noise performance severely because it is multiplied by the amplifier gain and summed to the total input capacitance. In addition, implementing the resistor with an active transistor allows us to vary the resistance value [3].

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The main amplifier consists of three stages: the gain stage, the level-shifting stage, and the output buffer stage. In the gain stage, the optimal transistor width for the input device, Z2, is chosen. Figure 3 shows circuit performance characteristics for different sizes of this transistor. The 3-dB frequency in Fig. 3(a) decreases because a large width of Z2 contributes to larger input parasitic capacitance through Cgs. In Fig. 3(b), the noise characteristic is shown. Based on this data, 100 μm is chosen as the width of the input transistor in our design. The size of the level-shifting diodes should be determined to satisfy the DC biasing point as well as the number of diodes. This can be implemented with a diode-connected transistor where the gate resistance is measured to be about 1200 Ω/μm. The output buffer consists of transistors Z5 and Z6. The sizes of these transistors are chosen to obtain low output impedance while retaining a large linear range for the output buffer.

In Fig. 2, the interconnection (A) is used to improve the circuit performance. In contrast, the conventional transimpedance amplifier uses the interconnection (B). Using interconnection (A) reduces the loss of gain in the second stage. From the simple model,

\[
\left| \frac{dV_{in}}{dI_{in}} \right| = \frac{R_f F(a)}{1 + sR_f C_T},
\]

\[
C_T = \frac{C_m + (1 + a A_v)C_p}{1 + a A_v},
\]

where \( A_v \) = gain of the first stage,
\( R_f \) = feedback resistance, \( F(a) \) = transimpedance factor,
\( a = dV_d/dV_p \),
\( C_T \) = parasitic capacitance of \( R_f \), and
\( C_m \) = \( C_{MOS} + C_{gd} \).

If interconnection (A) is used, \( F(a) = A_v/(1 + A_v) \). If interconnection (B) is used, \( F(a) = A_v(1 + A_v) \). The calculated results for transimpedance gain and bandwidth are shown in Fig. 4. The 3-dB frequency in Fig. 4(b) is the frequency at which the 3-dB degradation of the ideal transimpedance is obtained. When the gain across the diodes is less than 1, the new circuit can achieve larger transimpedance value compared with the conventional one without loss of the bandwidth. The feedback resistance value can be reduced to increase the bandwidth for the same transimpedance gain as long as the noise performance is within specifications. In the interconnection (B), the fluctuation on the ground line can be added to the output through the bias transistor Z4 and the connection (B). However, that noise cannot be added to the output in (A) because the noise cannot go through the level-shifting diodes in the reverse biased direction. In addition, the interconnection (A) can reduce capacitance loading at node 6. A summary of the SPICE-3CI simulation results is listed in Table 1.

III. Experimental Demonstration and Results

This integrated optical receiver circuit is to be used in the System Demonstration Projects of the DARPA-supported National Center for Integrated Photonic Technology to achieve phased-array radars and optical computing machines as shown in Fig. 5. Multiple copies of the optical receiver module are to be used in optical computing systems which utilize free-space interconnection. They are to be used in phased-array radars to achieve high-bandwidth communication.

Measured output characteristics of a depletion-mode MESFET with W/L = 40 μm/1.2 μm are shown in Fig. 6. SPICE parameters were extracted from such data and used for all calculations and simulations [4]. The measured transconductance per 1 μm width is 0.16 mA/V, while the simulation result is 0.185 mA/V. The measured output resistance is 4.49 kΩ, and the simulation result is 3.48 kΩ.

In Fig. 7, the DC voltage transfer curve of the amplifier is shown. A DC gain of about 10 is obtained with the ±5 V power supply.

Our prototype chip includes several copies of the optical receiver circuit with different transistor geometries, in order to characterize the performance of the receiver. In addition, an array of four optical receivers is to be used for the investigation of spatial resolution, power dissipation limitation, and the effect of crosstalk between channels. The layout of the optical receiver circuit is shown in Fig. 8. It occupies an area of 221.6 μm x 72 μm including an MSM photodiode. The die photo of the entire GaAs chip is shown in Fig. 9. An optical measurement system is being constructed which uses a laser diode with wavelength less than 0.85 μm and modulation rate higher than 1.0 GHz.

IV. Conclusion

A GaAs gigahertz optical receiver has been designed. The receiver has also been fabricated through the MOSIS service. Critical design factors to improve the performance of the receiver have been considered in our design. This optical receiver circuit is to be used in system level demonstration of integrated optoelectronic computing and interconnection.

Acknowledgment

The authors would like to thank Dr. S. R. Forrest for valuable discussions.

References

Fig. 1  Optical receivers and laser diodes used in optical computing and interconnection.

Fig. 2  Circuit schematic of the optical receiver. New interconnection scheme can be used to improve the performance.

Fig. 3  Circuit performance characteristics for different widths of the input transistor $Z_2$.
(a) 3-dB frequency.
(b) Equivalent input noise.

Fig. 4  Circuit performance characteristics for different interconnection schemes (A) and (B) in Fig. 2.
(a) Transimpedance gain.
(b) 3-dB frequency.
Fig. 5 An array of the optical receivers are used for the System Demonstration Projects of the Darpa-supported NCRIPT.

Fig. 8 Layout of the optical receiver.

Fig. 9 Die photo of the prototype chip fabricated through MOSIS service.

Fig. 6 Measurement results of a 40 μm/1.2 μm depletion-mode MESFET.

Table 1 SPICE simulation results of the optical receiver.

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