DESIGN CONSIDERATIONS FOR DIGITAL CIRCUIT INTERCONNECTIONS
IN A MULTILAYER PRINTED CIRCUIT BOARD

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ABSTRACT
The design considerations of signal lines in a multilayer printed circuit board are discussed. In particular, the effect of the orthogonal lines on the impedance, delay, and signal cross-talk is investigated for a single line and two coupled lines. Also discussed is the effect of loading and cross-over lines in the memory card design.

1. INTRODUCTION
In a computer system, to store or retrieve data from the memory, the central processing unit (CPU) generates the address of a particular memory location and places it on the memory bus, which is connected to the memory card design. These memory chips may supply data to the CPU or hold output data from the CPU or hold output data from the memory. The memory card design includes the signal line characteristic impedance, matched load impedance, and adjacent parallel signal line near-end and far-end cross-talk [3,4,5]. While designing a card for the memory application, one has to consider the chip capacitive loading, the effect of the orthogonal lines, and simultaneous switching of the parallel address lines. They affect the cross-talk, delay and desired output impedance of the driver circuit. Design guidelines to assess these effects and assist in the proper design of a memory card will be discussed.

In this paper, we shall present the above design considerations for two signal layers above the ground plane in a homogeneous medium in a card as shown in Figure 1. The signal lines on the layer closer to the ground are along the x-axis. We shall assume that the signal lines of interest run in the y-direction. They affect the cross-talk, delay and desired output impedance of the driver circuit. Design guidelines to assess these effects and assist in the proper design of a memory card will be discussed.

2. SINGLE SIGNAL LINE WITH CROSS-OVER LINES
Figure 2a represents a vertical cross-section of a stripline structure consisting of a signal line and cross-over lines imbedded in a homogeneous dielectric medium above a reference plane. The signal and the cross-over lines have with width W and Wx, respectively. Both lines are assumed to have the same thickness, T. As shown in Figure 2a, H is the height of the signal line above the ground plane and Hx is the separation of the signal line and the cross-over line in the vertical direction. The medium property is represented by the relative dielectric constant εt.

The capacitance (Ct) and inductance (L) of a signal line in absence of the cross-over lines can be estimated as described in [5] by

\[ C_0 = \varepsilon_t \frac{W}{H} \left( \frac{W}{H} \right) \left( \frac{W}{H} \right)^2 \]  

where \( C_0 = 9.5 \mu F/m \), \( W = W \), and \( H = H \).

The characteristic impedance (Z0) and the signal propagation delay (τ) can be expressed as

\[ Z_0 = \sqrt{\frac{LC_0}{W}} \]  

\[ \tau = \frac{1}{Z_0 C_0} \]

3. SINGLE SIGNAL LINE WITH CROSS-OVER LINES
Consider an example of Figure 2a with H/W=0.4, H/H=2, T/W=0.5, Wx=W, ε=4. For a single line, C0=95.7μF/m, L=0.4649μH/m, Z0=70Ω and τ=6.67ns/m. In the presence of the cross-over lines with periodicity, Pt=2W, Ct=145.0μF/m, ΔC=C0+Cx, Zx=56.62Ω, and τ'=8.21ns/m.

Numerical computations show that in the presence of the cross-over lines, the capacitance per unit length of the signal lines is increased. The characteristic impedance is decreased, and the delay per unit length of the line is increased. It is noticed that the cross-over effect becomes significant when the periodicity, Pt, is less than 4 times the line width.
3. TWO SIGNAL LINES WITH CROSS-OVER LINES

Consider two parallel signal lines of the same width with cross-over lines above the ground plane as shown in Figure 3a. The signal lines are separated by \( S \). The capacitance and the inductance matrices in the absence of the cross-over lines (see Figure 3b) in the homogeneous medium can be expressed as

\[
[C] = \begin{bmatrix}
C_{11} & C_{12} \\
-C_{12} & C_{22}
\end{bmatrix}
\]

where \( C_{11} \) is the self inductance of the line 1 and \( C_{22} \) is the self inductance of the line 2, and \( C_{12} \) is the coupling inductance. To calculate the self capacitance of the active line, the matched load impedance for terminations, the near-end and far-end of the signal lines is determined from [8] as

\[
C_{sl} = \frac{L_{sl}}{L_{11}} \mu H/m
\]

where \( C_{sl} \) is the short circuit or self capacitance and \( L_{11} \) is the inductance of the line 1 and \( L_{11} \) is the self capacitance for line 1 and \( L_{22} \) and \( L_{12} \) are the coupling capacitance (mutual inductance) between the two lines. The self capacitance is the sum of \( C_{11} \) and \( C_{22} \), i.e., \( C_{11} = C_{sl} + C_{11} \) (see Figure 3b).

In the presence of the cross-over lines, the dielectric medium becomes inhomogeneous because the cross-over lines behave like a dielectric medium with infinite relative dielectric constant. Numerical computations show that the self capacitance is increased significantly and the coupling capacitance decreases by decreasing the periodicity of the cross-over lines [5,6]. Thus, as shown in Figure 3c, the self capacitance \( C'_{11} \) becomes the sum of \( C_{11} \) and \( C_{11}' \), i.e., \( C_{11} = C_{11} + C_1' + C_{11}' \). \( C_{11} \) and \( C_{11}' \) can also be expressed as \( C_{11}' = C_{11} + \Delta C_s \), \( \Delta C_s = C_{11}' - C_{11} \), \( C_{11}' = C_1' + C_{11}' \), and \( \Delta C_s = C_{11}' - C_{11} \), where \( \Delta C_s \) and \( \Delta C_s' \) are positive and \( \Delta C_s > \Delta C_s' \). These changes are due to the cross-over capacitance as calculated using a 3-D capacitance program [6].

Capacitance measurements were also carried out to verify the calculated results. The simulated and measured results for capacitance are in good agreement and are given in Appendix-A.

3.1 MATCHED LOAD IMPEDANCE

The matched load impedance \( Z_{ML} \) for the coupled lines is defined as the output impedance of the active line so that the reflections can be minimized. The matched load impedance in the presence of the cross-over lines is determined from [8] as

\[
Z_{ML} = \frac{-L_{sl}^2 + \sqrt{L_{sl}^2 - 4C_{11}' \Delta C_s}}{2C_{11}' \Delta C_s - (C_{11}' - C_{11})^2}
\]

Figure 4 shows a plot of percentage change in the matched load impedance from the characteristic impedance of the signal line in the absence of the adjacent and cross-over lines as a function of \( H/S \) for \( P=2W_1 \), \( P=4W_1 \), and \( P=2W_1 \). The curves are shown for \( W/S = 1 \), \( H/H = 0.4 \), \( T/W = 0.5 \), and \( A = 4 \). It is noticed that the change in the matched load impedance is significant when periodicity of the cross-over lines is less than 4 times the line width.

3.2 CROSS-TALK

As shown in Figure 5a, line 1 is connected to an active signal with a source impedance equal to the matched load impedance and the near-end of line 2 and the far-end of line 1 and 2 are connected to their matched load impedances. Using the matched load impedance for terminations, the near-end and far-end of line 2 will have line voltages, called near-end and far-end cross-talk or coupled noises, due to an active signal on line 1. The ratio of near-end (far-end) coupled noise on line 2 to the active signal voltage is defined as the backward (forward) coupling coefficients, \( b_1 \) and \( b_2 \). The coefficients \( b_1 \) and \( b_2 \) are given as

\[
b_1 = \frac{1}{4} \left( \frac{C_{11} + \Delta C_s}{C_{11}' + \Delta C_s} \right) L_{sl}
\]

(8)

The term \( 0.25(\Delta C_s/C_{11}') \) is referred to as the capacitive coupling coefficient, and the term \( 0.25(\Delta C_s/C_{11}') \) is referred to as the inductive coupling coefficient. In the absence of cross-over lines, the medium is homogeneous and \( \Delta C_s=0 \) and \( \Delta C_s'=0 \). In this case, \( C_{11}/C_{11}' \) is equal to \( (L_{sl}/L_{11}) = a_1 = 0 \) and \( b_2 = 0.5(C_{11}'/C_{11}) \). Figure 6 shows a plot of capacitive coupling \( (C_{11}'/C_{11}) \) as a function of \( H/S \). Figure 4 shows that as the cross-over effect increases by decreasing the periodicity (P) of the cross-over lines, the capacitive coupling \( (C_{11}'/C_{11}) \) decreases. From Eq. (8), as P decreases, the forward coupling coefficient increases negatively and the backward coupling coefficient decreases . This reduces the near-end coupled noise and increases negatively the far-end coupled noise. One can also determine \( a_1 \) and \( b_2 \) by using Figure 4. For example, for \( P=2W_1 \), \( H/S = 1 \), \( W/S = 1 \), \( T/W = 0.5 \), \( W = W_2 \) and \( H = H_2 \), the ratio \( C_{11}'/C_{11} \) is 0.09 which is obtained by using curve for \( P=2W_1 \) and \( (L_{sl}/L_{11}) = 0.28 \) which is determined by using the curve of the active line. Thus the computed coefficients are \( a_1 = 0.0475 \) and \( b_2 = 0.0925 \).

For an example, an ASTAP simulation [12] for two coupled lines is carried out for the signal line length, \( d=0.3m \) and rise time, \( T_r=3ns \). Time, \( T_1=3ns \) with one signal line active and another signal line quiet as shown in Figure 5a. It is observed in Figure 5(b,c) that the near-end coupled noise decreases slightly and the far-end coupled noise has substantial negative increment as the periodicity of the cross-over lines decreases. This effect of coupled noise is significant when the periodicity of the cross-over lines is less than 4 times the line width.

3.3 SIGNAL PROPAGATION DELAY

Consider the effect of cross-over lines on the signal propagation delay. In a two coupled line case as shown in Figure 6a, both lines are active with source impedance equal to their matched load impedance and the near-end and far-end are terminated in their matched load impedances. The base of the near-end of line 1 and 2 would be \( (1+b_2)V_0 \), where \( 2V_0 \) is the source voltage. Thus the voltage on line 1 is no longer equal to \( V_0 \). Similarly, when line 1 is active with source voltage \( 2V_0 \) and line 2 is active with source voltage \( -2V_0 \), the voltage on line 1 and line 2 are \( (1+b_2)V_0 \) and \( -(1-b_2)V_0 \), respectively. When both lines are active with a positive source voltage, the common mode occurs. When one line is active with positive source voltage and the other line is active with negative source voltage, then the signal propagation occurs in the difference mode [2,5,13-15]. The velocity of signal propagation in the common and difference modes are \( \tau \) and \( \tau_2 \), respectively, for two coupled lines of symmetrical cross-section with cross-over lines. They can be determined as

\[
\tau_1 = \frac{\tau_1}{\tau_1 + L_{sl} \Delta C_s + \Delta C_s} \Delta C_s\Delta C_s (\text{ns})^2
\]

(9)

\[
\tau_2 = \frac{\tau_2}{\tau_2 + L_{sl} \Delta C_s + \Delta C_s} \Delta C_s\Delta C_s (\text{ns})^2
\]

(10)

\[
\tau_2 = \frac{\tau_2}{\tau_2 + L_{sl} \Delta C_s + \Delta C_s} \Delta C_s\Delta C_s (\text{ns})^2
\]

where \( \tau_2 \) is the propagation delay when the cross-over lines are not present.

Figure 6(b,c) shows the voltage waveforms at the near-end and far-end of the signal lines operating in the common mode and the difference mode with the far-end of the signal lines open for two cases (i) no cross-over (ii) with cross-over, \( P=2W_1 \) for line length, \( d=3m \) and rise time, \( T_r=3ns \). It is observed that, in this case, the common mode travels slower than the difference mode. The time difference between the common mode and the difference mode delay is zero in the no cross-over case and 0.552ns for \( d=3m \) resulting in 1.84ns/m.
in the cross-over case with P=2W1. These data are given in Table 1. This timing difference of 0.552ns accounts for the far-end noise illustrated in Figure 5c. Thus, as the effect of the cross-over lines increases, the time difference between the common mode and the difference mode increases and the far-end noise becomes more negative.

Figure 6(b,c) also shows the effect of cross-over lines on the common mode and difference mode voltages. The near-end voltage in common mode is 1.15V as opposed to the expected 1 volt as given in Figure 6c. In the difference mode, the near-end voltage is 0.85V. The ratio of the difference mode voltage to the common mode voltage is 0.75 for loaded and P=2W1.

The goal is to keep this ratio as close to one as possible to minimize noise immunity impact to the receiver circuit design [1,2,15]. The design is further complicated with the addition of cross-over lines and the associated capacitance changes discussed so far in this paper. Figure 7 shows a memory card with cross-over lines. Let's consider the effects of the cross-over lines on coupled noise, signal line propagation delay and the desired driver circuit output impedance for this structure.

Assume that in the memory card, the lines are loaded with ΔC, pF/m. In the presence of the capacitive loading, the self capacitance is increased significantly. There is no additional change in the mutual capacitance. The self capacitance C's will be equal to (C1+ΔC,1+ΔC2). Equations (7) to (10), described in Section 3, are valid if C's is replaced by C's11. In summary, the equations can be expressed as

\[ Z_m = \left( \frac{U_{11}^2 - L_{11}^2}{C_{11}^2 + \Delta C_1^2 + \Delta C_2^2 + \Delta C_{12}^2} \right)^{i/2} \]  

(12)

\[ h_{21} = \frac{1}{4} \left[ \frac{C_{12}^2 + \Delta C_1^2 + \Delta C_2^2}{L_{11}} \right] \]  

(13)

\[ \tau_1 = \frac{\Delta C_1}{2 \tau_{11}} \]  

(14)

\[ \tau_2 = \frac{\Delta C_2}{2 \tau_{11}} \]  

(15)

For an example as given in Table 2, memory chip capacitive loading (ΔC,1) of 50 pF/m, which is 52% of the self capacitance of the signal line, is assumed. Figure 8(a,b) shows the ASTAP transient simulation for this example. It is noticed that the effect of loading and cross-over lines reduces the near-end coupled noise and increases negatively the far-end coupled noise. Therefore, if the memory card has cross-over lines it cannot withstand the same loading as that without cross-over lines and still keep the same far-end coupled noise. The designer may decrease the capacitive loading or increase the spacing between signal lines to stay within the same far-end coupled noise allowance.

4. CROSS-OVER EFFECT ON MEMORY CARD DESIGN

A memory card has many parallel address lines connected to a number of memory chips. These memory chips add an additional capacitive load on the line. This capacitive load affects the coupled noise and signal line propagation delay and requires a reduction in the driver circuit output impedance [2,13,15]. The design is further complicated with the addition of cross-over lines and their associated capacitance changes discussed so far in this paper. Figure 6 shows a memory card design with cross-over lines. Let's consider the effects of the cross-over lines on coupled noise, signal line propagation delay and the desired driver circuit output impedance for this structure.

Now consider the effect of the cross-over lines and the capacitive loading on the signal propagation delay. Figure 9 shows the voltage at the near-end and far-end of the signal lines operating in the common mode and difference mode with far-end open circuited for cross-over with P=2W1 and loading of 50pF/m. The time difference between the common mode and difference mode is 2.59ns/m. Referring to Figure 6(b,c), the time differences are 0 and 1.84ns/m, respectively, for the cases (a) no cross-over and (b) with cross-over, P=2W1. The time difference between the common mode and the difference mode is crucial to understand in order for proper switching to occur [2,14,15]. In Figures 6(b,c) and 9, it is observed that there is a relatively small change in the difference mode delay, while the common mode delay changed more significantly. Therefore, memory cards with cross-over lines further complicate the timing problems faced by the design engineer. It can be noticed from Figure 9 that the ratio of the difference mode voltage to the common mode voltage is 0.75 for loaded and P=2W1.

5. CROSS-UNDER EFFECT VS CROSS-OVER EFFECT

In the above analysis, it was considered that the signal lines were along the y-direction as shown in Figure 1a. Now, we assume the signal lines are along the x-direction in the outside layer which is further away from the ground plane. In this case, the y-directed signal lines would be viewed as the cross-under lines as shown in Figure 10(a,b). The height of the signal lines above the ground plane would be H1, + H2, + T. The cross-under lines would be below the signal lines by H2. Since the height of the signal lines (H1) is greater than H2, the matched load impedance is higher in the cross-under case than cross-over case. As shown in Table 1 and 2, the matched load impedances are 58.24Ω and 49.81Ω respectively for two lines, (a) without loading and (b) with memory chip loading for the cross-under case when P=2W1.

Comparing the cross-over and cross-under cases in Tables 1 and 2, it is found that the near-end noise and the negative far-end noise increase significantly more in the cross-under case than the cross-over case for P=2W1. It is also determined that the time difference between the common mode and the difference mode delay is more in the cross-under case than the cross-over case. Because of this the far-end noise is higher in the cross-under case.

6. EFFECT OF SIGNAL RISE TIME IN MEMORY CARD DESIGN

In the transient simulations discussed so far, the rise time assumed was 3ns. Suppose the rise time of the input signal
reduces. How does this effect the near-end and far-end noise for a memory card design with cross-overs? Since the roundtrip time across the coupled line is larger than 3ns, the near-end noise reaches its saturated value. The major effect would be on the far-end coupled noise. Figure 11 shows the far-end noise for the various rise times with \( P=4W \) and capacitive loading of 50pF/m. The time difference between the common mode and difference mode delay is approximately 0.669ns. This difference should be much less than the rise time of the signal to minimize the far-end noise [8, 14]. When \( T_r \) is less than 0.669ns, as is the case when \( T_r=0.5 \) and 0.1ns, the far-end noise saturates at -485mV. This is undesirable and should be avoided by insuring that the difference between the common and difference mode delays is much less than the rise time of the input signal.

7. CONCLUSIONS

The cross-over effect is significant when the periodicity is less than four times the line width. For a single line, the characteristic impedance decreases and the signal delay increases. For two coupled signal lines, the cross-over effect decreases the matched load impedance, increases the signal delay, decreases the near-end coupled noise and increases negatively the far-end coupled noise. The time difference between the common mode and the difference mode delay is also increased in the cross-over case.

In a memory card design with loading of 50pF/m, which is 50% of the self capacitance of the signal lines, the matched load impedance decreases. The signal delay, far-end coupled noise and the time difference between the common mode and the difference mode delay increase. The near-end noise decreases in the memory card. A memory card with cross-over lines cannot withstand the same loading as without cross-over lines and maintain the same coupled noise. It is necessary to increase the edge-to-edge spacing, \( S \) or decrease the loading.

Comparing the effect of the cross-over lines and the cross-under lines for two coupled signal lines, it is found that the matched load impedance, signal delay, both the near-end and far-end coupled noise and the time difference between the common mode and the difference mode delay are more in the cross-under case than the cross-over case.

The rise time of the input signal should be greater than the time difference between the common mode and the difference mode delay in order to avoid the far-end coupled noise reaching its saturation value.

8. REFERENCES


APPENDIX-A

The measured and calculated capacitances for a single line and two coupled lines are given below for \( T/W_I = .375 \), \( S/W_I = 1 \), \( H_0/H_1 = .625 \), \( W_I = .0254m \) and \( \varepsilon_r = 1 \).

<table>
<thead>
<tr>
<th>Single line</th>
<th>Two lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P=4W )</td>
<td>( P=6W )</td>
</tr>
<tr>
<td>( C_{S0} )</td>
<td>27.95</td>
</tr>
<tr>
<td>( C_{S1} )</td>
<td>20.37</td>
</tr>
<tr>
<td>( C_{S2} )</td>
<td>18.11</td>
</tr>
<tr>
<td>( C_{S3} )</td>
<td>30.35</td>
</tr>
<tr>
<td>( C_{D0} )</td>
<td>21.85</td>
</tr>
<tr>
<td>( C_{D1} )</td>
<td>8.50</td>
</tr>
<tr>
<td>( C_{S0}^{+} )</td>
<td>41.98</td>
</tr>
<tr>
<td>( C_{S1}^{+} )</td>
<td>19.88</td>
</tr>
<tr>
<td>( C_{AB}^{+} )</td>
<td>5.47</td>
</tr>
<tr>
<td>( C_{AB} )</td>
<td>16.63</td>
</tr>
</tbody>
</table>

From the above table, we notice that the theoretical capacitance calculations are in agreement with the measurement results with 2-10%.
Figure 1: Printed circuit board. (a) Two signal layers in orthogonal directions, (b) Cross-section of three signal lines with orthogonal lines.

Figure 2: One signal line with cross-over lines (a) cross-section, (b) capacitive representation ($C' = C_{G1} + C_{G2}$).

Figure 3: Two signal lines with cross-over lines (a) cross-section, (b) capacitive representation without cross-over lines ($C_{AB} = -C_{11}$, $C_{12} = C_{G1} + C_{AB}$, for symmetrical cross-sections, $C_{10} = C_{G0}$), and (c) capacitive representation of two signal lines with cross-over lines (for symmetrical cross-section, $C_{10} = C_{G0}$ and $C_{10} = C_{G0}$).

Figure 4: Capacitive coupling and matched load impedance as function of $H_2/S$ for $W_2/S = 1$, $H_2/H_1 = 0.4$, $T/W_1 = 0.5$, $\varepsilon_r = 4$, $P = \infty$, $P = 25W_1$, $P = 4W_1$ and $P = 2W_1$. 
Figure 5: Transient simulation: (a) schematic representation of two coupled lines, (Vs=2V), (b) near-end coupled noise and (c) far-end coupled noise for Wl/S=1, H1/S=2, Hx/H1=0.4, T/W1=0.5, ε=4, P=∞, P=25W, P=4W1, and P=2W1. Tr=3ns, length of the line, d=.3m.

Figure 6: Signal propagation delay: (a) schematic representation of two coupled lines; common mode (Vs=(2,2)) vs. difference mode (Vs=(2,-2)) for (b) no cross-over (P=∞) and (c) cross-over (P=2W) with far-end open circuited for Wl/S=1, H1/S=2, Hx/H1=0.4, T/W1=0.5 and ε=4. (Vcm: Common mode voltage, Vdm: Difference mode voltage)

Figure 7: Memory card with cross-over lines
Figure 9: Signal propagation delay in memory card: common mode \((V_s=(2,2))\) vs. difference mode \((V_s=(2,-2))\) for cross-over \((P=2W_1)\) with far-end open circuited for \(W_1/S=1, H_1/S=2, H_x/H_1=0.4, T/W_1=0.5, \epsilon_x=4, P=4W_1\), loaded with 50pF/m, \(\tau_r=3\)ns, length of the line, \(d=3m\).

Figure 8: Transient simulation for memory card: (a) near-end coupled noise and (b) far-end coupled noise for \(W_1/S=1, H_1/S=2, H_x/H_1=0.4, T/W_1=0.5, \epsilon_x=4, P=25W_1, P=4W_1\) and \(P=2W_1\), loaded with 50pF/m, \(\tau_r=3\)ns, length of the line, \(d=3m\).

Figure 10: (a) cross-over case: first layer has signal lines, (b) cross-under case: second layer has signal lines \((H'_1=H_1+T+H_2)\).

Figure 11: Signal rise time effect on the far-end coupled noise for memory card for \(W_1/S=1, H_1/S=2, H_x/H_1=0.4, T/W_1=0.5, \epsilon_x=4, P=4W_1\) and capacitive loading of 50pF/m, \(\tau_r=3, 2, 1, 0.5, 0.1\)ns.

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