The Architecture of the LR33000:
A MIPS Compatible RISC Processor for Embedded Control Applications

LSI Logic Corporation
1525 McCarthy Boulevard
Milpitas, CA 95035

Abstract

RISC processors have been widely accepted in the performance driven segments of the reprogrammable computer market such as workstations and file servers. However these chips, despite their high levels of performance, do not adequately address embedded control applications. This paper describes the macro- and micro-architecture of the LR33000 - a single chip, 50MHz, RISC processor which was designed and optimized for embedded control applications while retaining both software compatibility with the MIPS-1 instruction set and a high level of performance. The optimization for embedded control applications was done by focusing on the following goals: minimizing the overall system cost by increasing the level of integration, simplifying the system design, and reducing the power consumption.

1 Introduction

RISC processors have been widely accepted in the performance driven segments of the reprogrammable computer market such as workstations and file servers. This widespread acceptance has been driven by their significant performance advantage over CISC processors. Achieving this performance usually requires a sophisticated memory subsystem in order to sustain the required instruction and data throughput. There are several embedded control applications (such as laser printers, disk controllers, robotics, etc.) that require similar levels of performance. However these systems have somewhat different characteristics from general purpose computers. Most embedded applications are extremely sensitive to the overall system price and thus cannot use an expensive memory subsystem. They typically do not require virtual to physical memory translation and except for specific areas do not require, or can do without, floating-point arithmetic. Additionally some embedded applications tend to be very sensitive to power dissipation and interrupt latency. These characteristics make the use of standard RISC microprocessors less attractive for embedded control applications.

This paper describes both the macro- and the micro-architecture of the LR33000 - a single chip, 50MHz, RISC processor which was optimized for embedded control applications while retaining both software compatibility with the MIPS-1 instruction set [1], and a high level of performance. The optimization for embedded control applications was done by focusing on the following goals: minimizing the overall system cost by increasing the level of integration, simplifying the system design, and reducing the power consumption.

2 Microarchitecture

Figure 1 shows a block diagram of the chip. It is composed of five major blocks: a MIPS-1 compatible CPU core, an 8K byte instruction cache, a 1K byte data cache, a flexible memory controller, and three timer-counters. The following sections elaborate on each of these blocks.

2.1 CPU Core

The CPU core is the heart of the LR33000 processor. It has a five stage pipeline which is similar to that of the LR3000, and is software compatible with the MIPS-1 instruction set. Different pipeline structures and pipeline depths were evaluated at the beginning of the project. The decision to adopt a five stage pipeline was driven by the following two reasons: it was a good match for the target 1 micron drawn (0.7 micron effective) cell based technology, and it simplified maintaining software compatibility with the LR3000.

The only programmer visible architectural differences between the LR33000 core and the LR3000 are limited to
the system control coprocessor (CPO). These occur only in
supervisor mode and relate to necessary system management
issues, specifically memory management, cache control
and debug enhancements. Since the LR33000 does not
support memory management, the TLB and its associated
registers (Index, Random, EntryHi/Lo, and Context) have
not been implemented. Using any of the MMU instruc-
tions or referencing any of these registers will cause a soft-
ware trap.

The software breakpoint instructions of the LR3000
have been augmented by hardware breakpoints and an in-
struction trace facility. These features were added to aid
software development and the debugging of embedded
systems. The hardware breakpoints can be selectively in-
voked by both instruction execution and data read or write
accesses. The trace facility is used for tracking all the non-
sequential instructions executed by the program. In order
to support these features three registers have been added to
CPO. These are the Breakpoint on Program Counter (BPC)
register, the Breakpoint on Data Access (BDA) register,
and the Debug Control Register (DCR).

2.2 Caches

In order to reduce the overall cost and design complexity
of the embedded system the LR33000 chip has two inte-
grated on-chip caches. The instruction cache is 8K bytes,
whereas the data cache is 1K bytes. For a very wide range
of embedded control applications these caches are suffi-
ciently large to provide an attractive hit rate, thus obviating
the need for high speed external caches.

The on-chip caches are direct mapped, write-through,
with a line size of 16 bytes, and a valid bit per word. In or-
der to customize their use to the application several user
configurable modes are available. These modes include
the support of a configurable refill size, bus snooping, con-
trol over caching on a per access basis, disabling the cach-
es, and supporting direct access into and out of the caches.

A significant performance increase can be realized if the
cache refill size is fine tuned to the application. This is
demonstrated in figure 2 by changing the instruction cache
fill size for a 33MHz system running the Dhrystone bench-
mark. The LR33000 chip facilitates this by providing indi-
vidually configurable (from 4 to 64 bytes) block refill sizes
for both the instruction and the data accesses. Bus snoop-
ing was implemented to support multiprocessing and DMA
applications. When snooping is activated the LR33000 chip monitors all transactions on the external bus
and invalidates the internal cache entries that correspond
to addresses that are modified in main memory. The con-
trol over caching on a per access basis can be used to en-
sure that critical code segments may be locked into the
cache. Having the capability to disable the caches simpli-
ifies the system debug process by providing a means of
monitoring exactly what the CPU is accessing and execut-
ing.

2.3 External Memory Interface

A large portion of the system cost in embedded control
applications is determined by the memory subsystem. Con-
sequently having a flexible memory interface is extremely
important for embedded controllers. The LR33000 chip
supports two independent memory protocols: a DRAM
mode, and a Synchronous mode. These modes are mapped
to separate memory regions and can be used independently
to access different sorts of memory. They were de-
designed to enable a clean interface with several types and
speeds of memory with minimal external glue logic.

The DRAM mode was defined to work directly with
commercially available page mode DRAMs (using CAS
before RAS refresh). The LR33000 chip directly generates
the RAS and CAS signals for the memory address strobes
and the select strobe (DMXSEL) for the row and column
addresses. This provides the system designer with the flex-
ibility of using several commercially available DRAM
configurations. The LR33000's timing specifications are
such that in a 40MHz system 70ns DRAMs can be used,
whereas at 33MHz only 80ns DRAMs are required. Using
this mode, block accesses typically consist of a four cycle
access for the first word, and only two cycles per each ad-
ditional word. It is possible to achieve higher performance
by utilizing single cycle burst mode if the memory sub-
system is capable of supporting the higher throughput (e.g.
by using interleaved memory). It is also possible to access
slower memories by programming the LR33000 to widen
the CAS width strobe and the RAS precharge time, or by
inserting additional wait states per memory transaction.
The internal refresh counter can be used in conjunction
with the on-chip DRAM controller to generate the refresh
sequences and obviate the need for any external DRAM
control.

The Synchronous mode connects directly with 32 bit
SRAMs, ROMs, EPROMs, and provides the hooks for ac-
cessing more specialized memories such as static column
DRAMs, etc. The early memory transaction start signal
(MXSTART) together with the block fetch request signal
(BFREQ) can be used to predecode the high order bits of
the address bus and to support block fetches. The basic
memory transaction in this mode is two cycles long.

An additional mode was defined specifically for booting
or otherwise accessing 8 bit devices. In this 8-bit mode the
LR33000 chip initiates four byte accesses for every mem-
ory word read and does the byte gathering on-chip. In addi-
tion it is possible to program (through the use of an internal
register) the number of wait states used in this mode and to
further reduce the amount of external logic required. The
external EPSEL and IOSEL decode signals are activated
whenever the chip generates accesses to the memory mapped PROM and IO regions of memory respectively and can be connected directly to the memory chip select input thereby reducing the number of external devices.

2.4 Counter-Timers

Most embedded applications need a set of counter-timers for real time control. The LR33000 chip has three counters which are memory mapped together with their corresponding control registers. Two of the counters (Timer1 and Timer2) are 24 bit memory mapped down counters which can be synchronously accessed, started and stopped. They are both connected to the internal interrupt ports and generate an interrupt when they count down to zero. In addition the input clock for Timer2 as well as its zero detect signal are connected to external pins. Consequently it can be used as an external event counter as well as providing an external indication of a count of zero. The third counter (RCOUNT) is a 12 bit down counter which was defined to support DRAM refresh. Its output can be connected either to the internal DRAM controller or to an external one in order to initiate refresh sequences.

3 Performance

The SPEC benchmark suite has become the most widely accepted criterion for comparing microprocessors' performance in a workstation/server environment. Unfortunately a similar suite of benchmarks does not exist for embedded control applications. Moreover due to the huge diversity of these applications the availability of such a tool would probably be considerably less useful.

In this section we have used the Dhrystone benchmark as the vehicle for comparing various system level tradeoffs in using the LR33000 chip. The intent was not to demonstrate what peak performance an LR33000 based system can achieve with the fastest (i.e. most expensive and therefore unrealistic for embedded control) memory. Rather the goal was to show the range of performance using a very basic (and low cost) memory subsystem and to show how it can be improved upon by using a faster memory subsystem.

Figure 2 demonstrates the effects of using different block refill sizes for the I-cache, assuming the same sort of memory subsystem. For this application, a block refill size of 16 bytes is optimal and yields the highest performance.

Figure 3 demonstrates the performance advantages of supporting single cycle burst refill mode vs. the dual cycle option on the Dhrystone benchmark. It should be noted that at 40 MHz the LR33000 processor only requires 70ns DRAMs to support the dual cycle refill mode. At lower frequencies it is possible to use faster DRAMs and support single cycle burst refills, whereas at higher frequencies an interleaved memory subsystem is probably required. Both of these options require a more expensive memory subsystem but can deliver significantly higher performance.

4 Implementation Technology

The LR33000 die is 12.7mm on a side and consists of close to 700,000 transistors. It was implemented in a 1 micron drawn, 0.7 micron effective channel length, double metal cell based technology using a standard cell ASIC tool suite throughout all phases of the design. The static cell based technology and design environment were chosen in order to achieve a fast and compact design while retaining the quick design cycle associated with the ASIC methodology [2]. The project took less than a year from product definition to first silicon which was fully functional [3].

Several speed grades are available, spanning the range from 25 to 50MHz, with power dissipation of 2-4W respectively. The lower speed versions of the chip are packaged in both 155 pin CPGA, and 160 pin PQFP versions, with the higher frequency and power versions initially planned for release in a CPGA.

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References

Figure 1: The LR33000 Block Diagram

Figure 2: Different I-Cache Block Fill Size Effects

Figure 3: Single Cycle vs. Dual Cycle Refill