F-RISC/G: AlGaAs/GaAs HBT Standard Cell Library

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Abstract
A standard cell library for implementing Rensselaer's Fast Reduced Instruction Set Computer (F-RISC/G) project with Rockwell's AlGaAs/GaAs Heterojunction Bipolar Transistor (HBT) technology is presented. The processor is targeted at an instruction cycle time of 1.0 ns. Differential Current Mode Logic (CML) is used, and unloaded gate delays are 15-20 ps.

1 Introduction
A key goal of the Fast Reduced Instruction Set Computer (F-RISC/G) project is to achieve an instruction cycle time of 1.0 ns. F-RISC/G uses an advanced, highly pipelined architecture to help attain this goal. However, the architecture alone cannot meet the speed criteria without an exceptionally fast circuit technology. Rockwell's AlGaAs/GaAs HBT process has been chosen for F-RISC/G. A crosssection of their HBT device is shown in figure 1.

An interesting comparison can be made between Rockwell's HBT and other high-speed technologies. For example, a related project (F-RISC/I [1]) is intended for the Vitesse MESFET process, which has higher integration levels and allows a single chip implementation. Power is lower for the MESFET version, but the cycle time of the processor is twice as long. Table 1 shows a brief comparison of three different process technologies: the Tektronix Advanced Silicon Bipolar, used in the F-RISC/E project [2]; the Vitesse 1.2μm MESFET; and the Rockwell HBT.

The F-RISC/G gate library includes both Current Mode Logic (CML) gates and Emitter Coupled Logic (ECL) gates. Each gate uses differential logic and can have up to three levels of current switches. ECL gates consist of a CML gate connected to an emitter follower. The emitter follower shifts the output voltage in multiples of the transistor base-emitter voltage (VBE).

2 Circuits
A current switch (CSW) is the basic building block of all of the gates in the library. The input current into the common emitter node is switched left or right, depending upon the two base voltages. Since a full current tree with three levels of CSWs forms a three-to-eight decoder, any Boolean function of three variables can be implemented in a single current tree by using collector dotting at the top level. By eliminating CSWs with both collectors connected together and by using collector dotting at level two for intermediate decoding states, an efficient logic implementation is obtained. A four-input multiplexor gate is shown in figure 2.

Differential logic was chosen for F-RISC/G for speed and common mode noise rejection. However, differential logic has disadvantages. Circuit area is increased as both a signal and its complement need to be wired. No commercial routers can ensure that differential signals are routed next to each other. For the target 1.0 ns machine, the speed increase outweighs these disadvantages.

Differential signals can be inverted with zero delay and power by exchanging the true and the inverted

Table 1: Technology Comparison.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>HBT</th>
<th>MESFET</th>
<th>Si Bipolar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>19 ps</td>
<td>74 ps</td>
<td>90 ps</td>
</tr>
<tr>
<td>Power</td>
<td>14 mW</td>
<td>0.6 mW</td>
<td>10 mW</td>
</tr>
<tr>
<td>Gates (equiv)</td>
<td>1000</td>
<td>50000</td>
<td>3000</td>
</tr>
</tbody>
</table>

Figure 1: Crosssection of Rockwell HBT.
connections at any input or output port. Thus the standard cell library can be smaller since dual gates like AND and OR are physically identical. Figure 3 shows the circuit for a differential two-input AND/OR gate with two levels of series gating. The input signals for current switches at different levels must be offset by at least one base emitter junction voltage, $V_{BE} \approx 1.4V$, to avoid saturating the bipolar devices. For example, inputs to second-level CSWs are generated by ECL gates with an emitter follower which drops the output level by one $V_{BE}$.

To obtain the same noise margin as in differential logic, the single-ended logic needs twice the output voltage swing. Twice the voltage swing is sufficient, despite the fact that the generation of the reference voltages is sensitive to supply voltage drops on power rails, because doubling the voltage swing also doubles the maximum gain of the current switch [2].

Using SPICE models provided by Rockwell for the transistors, CML and ECL gates have been simulated. Figure 4 shows the switching characteristics of the AND/OR gate shown in figure 3. Figure 5 shows the delay of a CML gate as a function of its switching current. The delays are for the top-level input. The propagation delays from lower level inputs are longer. Also, for ECL gates there is an added delay through the emitter follower.

Each gate in the library is implemented in three power versions to allow flexibility for the designer. Medium and High power gates have unloaded delays below 20 ps and are used for general applications. Low power gates are used for less critical signals.

The primary performance difference between High and Medium power gates is in their sensitivity to load
A plot of the load sensitivity vs. switching current is given in figure 6. A push-pull amplifier with a lower sensitivity to load capacitance is used for applications such as driving clock lines. [2]

### 3 Layout

The HBT technology puts several limitations on the layouts of the standard logic cells. The collectors of the transistors must have the same orientation (i.e., collector contacts must be parallel to each other [3]). Since the metal contacts are located at various depths from the wafer surface, the interconnect metal step coverage presents another potential problem.

High speed cells on the critical path have high current levels. To avoid large voltage drops or electromigration, the power rails must be wide. Figure 7 shows the worst case voltage drop on the power bus as a function of power bus width for a typical high power gate. For a 40μm power rail, a worst case drop of 20 mV is seen. Since both the power rail and the ground rail are affected by the 20 mV drop, the supply voltage is reduced by 40 mV.

However, the increased width of the power bus has a detrimental impact on the gate performance because the capacitance between the power bus and a wire running under it is increased. This effect is more significant in GaAs technologies because the capacitance to
the semi-insulating substrate is negligible.

To reduce power dissipation and cell area, the current source transistor is replaced with a resistor in F-RISC/G standard cells. This allows the chip power supply to be reduced by \( V_{BE} \). For single-ended logic, the resistive source is more susceptible than the active source to power supply noise. However, this effect is not expected to be as severe for differential logic. Also, on-chip bypass capacitors on the power rails can be used to reduce noise. The issue will be resolved by testing sample circuits.

Figure 8 shows the layout of the two-input AND/OR gate. The power and ground rails are 50\( \mu \)m wide for a worst case voltage drop of 35 mV. The total cell area is \( 72\mu m \times 177\mu m = 12744\mu m^2 \).

4 Conclusion

The Rockwell AlGaAs/GaAs HBT process appears fast enough for implementation of the F-RISC/G processor. Simulations of some small subcircuits made from the standard cell library suggest that the 1.0 ns goal can be met.

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References


