A LOW-IMPEDANCE LOAD DETECTOR CIRCUIT FOR OPTICAL INTERCONNECTS

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ABSTRACT

Optical interconnects is a possible alternative for long distance electrical clock distribution in high-speed VLSI circuits. In an optical interconnect system, the response of the detector circuit is an important factor in determining the speed of the overall system. A simple low-impedance nMOS detector circuit is presented and modeled for optical interconnect application in CMOS systems. A maximum-current parameter is also defined and optimized to improve the circuit response. For 0.5-mW optical input power and a 25-μm diameter detector, response times of 2.2, 1.1 and 0.8 ns can be achieved respectively with typical 2, 1 and 0.5-μm technologies. With higher optical power or a smaller detector diameter, the response is faster. Analytical results, SPICE simulations, and preliminary experimental results are illustrated and discussed.

I. INTRODUCTION

Optical interconnects has recently been presented as a method to improve the performance of VLSI systems [1]-[5]. In an optical interconnect system, the response of the detector circuit is an important factor in determining the speed of the overall system. Many researchers have investigated the application of optical interconnects in CMOS systems, and realized prototypes [6]-[13]. However the operation speed of these systems was low [7]-[11], and was attributed to the slow response of the detector circuits.

The speed of a switching circuit is determined by the sum of the rise and fall times, which is defined as the total switching time in the following discussion. A high-speed computing system requires both minimum switching rise and fall times. In order to obtain a symmetric waveform in a CMOS circuit, the aspect ratios (gate width/length ratios) of two complementary transistors are adjusted to compensate for the difference between electron and hole mobilities. In an optical interconnect system, the rise and fall times, as well as the output logic swing of the detector circuit are controlled by the photocurrent and biasing conditions. To minimize the total switching time of the detector circuit with a full logic swing, both the photocurrent and the biasing load must be considered.

The basic detector circuit and its equivalent representation in a CMOS system are shown in Fig. 1. In the figure, $V_{DD}$ is the supply voltage, $V_o$ is the output voltage, $C_T$ represents the total effective capacitance (which includes CMOS inverter input capacitance, the detector capacitance and the biasing load device output capacitance), $I_{ph}$ is the photocurrent of the detector during an illumination pulse, $I_L$ is the load current, and $I_{C_T}$ is the capacitor current. Both the rise and fall times are functions of the type and magnitude of the load. When a light pulse illuminates the detector, a photocurrent $I_{ph}$ is generated and is divided between $I_L$ and $I_{C_T}$. A smaller load with a larger $I_L$ decreases $I_{C_T}$ and requires a longer time to charge the capacitor to a desired voltage level. When the light is turned off, there is no photocurrent and the load current $I_L$ discharges the capacitor. A smaller load will have a higher discharging current $|I_{C_T}|$ and a shorter fall time. By adjusting the effective load resistance, the average capacitor charging and discharging currents can be equalized, providing a symmetric clock waveform with equal rise and fall times. In this case, the total switching time is minimized.

II. LOW-IMPEDANCE LOAD DETECTOR CIRCUIT

In our circuit, an enhancement-mode nMOS transistor is used as the biasing load. The two basic structures are shown in Fig. 2. Previous researchers have investigated
the saturation structure shown in Fig. 2(a), in which the gate is connected to the drain (VGS = VDS), and shown the slow switching response [7]-[11]. In this configuration, the average charging current is always greater than the discharging current such that the falling response has a long tail. Typical I-V characteristics and switching response are shown in Fig. 3. A detailed analysis of this circuit was discussed in another paper [14].

Here, the low-impedance structure shown in Fig. 2(b) is presented for high-speed operation. In this configuration, VGS = VDD and VGS = VDS, which biases the gate to the most positive potential to keep the transistor in the on-state with a low effective channel resistance. The drain saturation voltage is given by

\[ V_{DSS} = V_{DD} - V_T, \]  

and the drain saturation current is given by

\[ I_{DS} = \frac{1}{2} k V_{DSS}^2, \]  

where \( V_T \) is the threshold voltage. Fig. 4 shows the typical I-V characteristics of this circuit. To have a full output logic swing, the saturation current I_DS must be smaller than \( I_{ph} \). To model this circuit, a maximum-current parameter \( m \) is defined describing the relation between the photocurrent and the maximum device current, where

\[ m = \frac{I_{ph}}{I_{DS}}. \]  

When a light pulse illuminates the detector, a photocurrent \( I_{ph} \) is generated and charges the capacitor \( C_T \). Before the output voltage \( V_o \) is charged to the level of \( V_{DSS} \), the transistor operates in the triode region and the drain current is

\[ I_D = k \left( V_{DSS} V_o - \frac{V_o^2}{2} \right). \]  

The time for \( V_o \) to charge from 0 V to \( V_{DSS} \) can be solved and is given by [14]

\[ t_{r1} = \frac{m V_{DSS}}{\sqrt{m - 1} I_{ph}} C_T \tan^{-1}\left(\frac{1}{\sqrt{m - 1}}\right). \]  

When \( V_o \) reaches \( V_{DSS} \), the transistor operates in the saturation region and the drain current is constant (I_DS). The time for \( V_o \) to charge from \( V_{DSS} \) to 0.9V DD is

\[ t_{r2} = \frac{m (0.9 V_{DD} - V_{DSS})}{(m - 1) I_{ph}} C_T. \]  

The rise time \( t_r \) for \( V_o \) to charge from 0 V to 0.9V DD is the sum of \( t_{r1} \) and \( t_{r2} \), and is given by

![Fig. 2 Detector circuit with: (a) a saturation load (VGS = VDS); (b) a low-impedance load (VGS = VDD).](image-url)
0.10
0.08
I
2
9.5
12
8
6

0.00
0.02
0.04
0.06
0.08
0.10
0.12
0.14

CURRENT (mA)

OUTPUT VOLTAGE (V)

Fig. 4 I-V characteristics of the low-impedance load. - - - : transistor. - - - - detector.

\[
t_r = \left\{ \begin{array}{ll}
0.9 \\
(m - 1) + \frac{1}{\sqrt{m - 1} \tan^{-1}\left(\frac{1}{\sqrt{m - 1}}\right)} \\
- \frac{1}{m - 1} \frac{V_{DSS}}{V_{DD}} \frac{mV_{DD}}{I_{ph}} C_T.
\end{array} \right.
\]  

(7)

If the illumination is turned off when the output voltage is at high-state, photocurrent goes to zero and the transistor current starts to discharge the capacitor \( C_T \). Before the output voltage \( V_o \) is discharged to the level of \( V_{DSS} \), the transistor operates in the saturation region and the time for \( V_o \) to drop from \( V_{DD} \) to \( V_{DSS} \) is

\[
t_{f1} = \frac{m(V_{DD} - V_{DSS})}{I_{ph}} C_T.
\]  

(8)

When \( V_o \) is discharged to the level of \( V_{DSS} \), the transistor again operates in the triode region. The time for \( V_o \) to drop from \( V_{DSS} \) to 0.1\( V_{DD} \) can be solved and is given by

\[
t_{f2} = \frac{mV_{DSS}}{2I_{ph}} C_T \ln(20) \left( \frac{V_{DSS}}{V_{DD}} - 1 \right).
\]  

(9)

Therefore, the fall time for \( V_o \) to drop from \( V_{DD} \) to 0.1\( V_{DD} \) is the sum of \( t_{f1} \) and \( t_{f2} \), and is given by

\[
t_f = \left[ (1 - \frac{V_{DSS}}{V_{DD}}) + \frac{V_{DSS}}{2V_{DD}} \ln(20) \left( \frac{V_{DSS}}{V_{DD}} - 1 \right) \right] \frac{mV_{DD}}{I_{ph}} C_T.
\]  

(10)

Using \( V_{DD} C_T/I_{ph} \) as the normalization time, the normalized rise and fall times are only functions of \( V_{DSS}/V_{DD} \) and the maximum-current parameter \( m \). To minimize the total switching time, the rise and fall times are equalized, which gives the following transcendental equation for \( m \):

\[
t_f = \left\{ \begin{array}{ll}
0.9 \\
(m - 1) + \frac{1}{\sqrt{m - 1} \tan^{-1}\left(\frac{1}{\sqrt{m - 1}}\right)} \\
- \frac{1}{m - 1} \frac{V_{DSS}}{V_{DD}} \frac{mV_{DD}}{I_{ph}} C_T.
\end{array} \right.
\]  

(7)

Since \( V_{DSS} = V_{DD} - V_T \), optimized values for \( m \) with different values for \( V_T/V_{DD} \) can be obtained with Eq. (11).

Based on a compatible CMOS process, the feature-size transconductance \( k_0 \) and the threshold voltage \( V_T \) are determined. For a desired operation voltage \( V_{DD} \), and a specific optical input power, the device aspect ratio \( W/L \) can be used as a design parameter to obtain the optimized \( m \) value from Eq. (11). The relation is given by

\[
I_{DS} = k_0 \frac{W}{L} \left( \frac{V_{DD} - V_T}{2} \right)^2 = \frac{I_{ph}}{m}.
\]  

(12)

where \( W \) is the gate width and \( L \) is the channel length of the transistor.

III. ANALYTICAL RESULTS, DESIGN EXAMPLES, AND PRELIMINARY EXPERIMENTS.

From the previous discussion, it was shown that the normalized rise and fall times are only functions of \( V_T/V_{DD} \) and \( m \). Results for different \( V_T/V_{DD} \) and \( m \) are illustrated in Fig. 5. It is very clear that the rise and fall times of this circuit can be equalized such that the total switching time is minimized. Optimized values for \( m \) with different \( V_T/V_{DD} \) can be solved from Eqs (11), and the corresponding normalized response time determined from (7) or (10), which are illustrated in Fig. 6. When \( V_T/V_{DD} \) varies by \( \pm 3\% \), the optimized \( m \) value changes by only \( \pm 3\% \) and the normalized response time by \( \pm 1\% \). Using typical values for \( V_T/V_{DD} = 0.15 \) in Fig. 6, when \( m \) varies from the optimized value by \( \pm 5\% \), the total switching time \( (t_r + t_f) \) changes by only \( +0.15\% \) and -0.5\%. Therefore, when the circuit is optimized, the sensitivity of the total switching
time to the variation of \( V_T/V_D \) is very low which gives a greater fabrication tolerance for the design.

Using typical 2-\( \mu \)m CMOS process and 5-V supply voltage as an example, \( V_T = 0.15V_D \), the inverter capacitance is 10.5 fF, the nMOS transistor output capacitance is 5.2 fF (with \( 2 \times 10^{14} \) epi-layer doping concentration) [15, 16], and the detector efficiency is 40%. When illuminated with 0.5-mW optical input power at a 780-nm wavelength, the photocurrent is 0.126 mA. For \( V_T = 0.15V_D \), the optimized \( m \) is 1.46 and the corresponding response time is 2.2 ns. For this CMOS process, a typical \( k_0 \) is 52 \( \mu A/V^2 \), and the value of 0.184 for the aspect ratio gives the desired 9.5 \( \mu A/V^2 \) for \( k \). A device with 2-\( \mu \)m gate width and 10.9-\( \mu \)m channel length can meet this requirement.

Once the circuit is optimized, the response time is determined by the detector photocurrent and size. The photocurrent is determined by the optical input power and the detector efficiency. The detector efficiency can be expressed by \( 1 - \exp(-\alpha d) \), where \( \alpha \) is the light penetration depth, which is 10 \( \mu \)m in silicon for 780-nm wavelength, and \( d \) is the junction depletion width. Assuming that the feature size scales as \( 1/S \), and the supply voltage by \( 1/V \) [17], the required optical input powers for different response times with 2, 1, and 0.5-\( \mu \)m technologies are shown in Fig. 8. For 0.5-mW optical input power, 2.2, 1.1 and 0.8-ns response can be achieved respectively. When the optical input power is higher or the detector size is reduced, the response is faster. From this information, the fan-out limitation of an optical signal distribution can be estimated to design an efficient interconnect system.

In our preliminary experiments, discrete devices (PIN-HS020 high-speed Si photodetector from United Detector Technologies and MM74HC04 high-speed CMOS inverter from National Semiconductor) were used. For these devices, \( V_D = 1.5 \) V, \( V_T = 0.6 \) V, \( I_{ph} = 3 \) mA, and \( C_T = 30 \) pF. Fig. 9 shows the switching response of two different
Fig. 9 Experimental response: (a) the saturation load; (b) the low-impedance load.

The falling response of the saturation structure produced a very long tail. The optimized low-impedance structure had a symmetric waveform with a response time of 50 ns, which is a significant improvement over the 4-ps fall time of the saturation structure.

In an integrated circuit with 30-fF capacitance, the capacitance can be reduced by three orders, and a 1-ns response for 20 fan-out with the same optical power is expected.

IV. CIRCUIT EXTENSION

The on-state output level higher than the supply voltage shown in Fig. 7 and 9 results from slightly forward biasing of the detector. To remove this unnecessary overcharge, one diode can be added between the power supply and the detector for a level-shift.

Since the response time is proportional to \( V_{DD}C_T/1_{ph} \), with an additional low-gain stage the logic swing of the detector stage can be reduced to further improve the performance. In this case, the logic swing is substituted by a smaller \( V_H \), which is the on-state output of the detector stage, and the gain \( G \) is \( V_{DD}/V_H \). When the required gain \( G \) is low, the response speed can be high from the basic gain-bandwidth-product characteristics, which will not increase additional delay. Distribute a fixed amount of optical power, the power required by each detector for the same operation speed can be reduced by a factor of \( G \), and a factor of \( G \) improvement in fan-out can be realized. If the optical input power keeps unchanged for the same fan-out, then the response speed can be improved by a factor of \( G \).

To have a lower \( V_H \) of the detector stage for this structure, additional diodes in series can be added between the power supply and the detector. For \( n \) diodes, \( V_H \) is obtained by

\[
V_H = V_{DD} - (n - 1)V_D,
\]

where \( V_D \) is the diode on-voltage. SPICE simulation response for different numbers of diodes with the same parameter values used above is shown in Fig. 10. Detailed analysis and design will be presented in another paper.

V. CONCLUSION

The analysis and experiments show that by optimizing a current parameter the low-impedance load detector circuit can provide high-speed optical interconnects in CMOS systems. The optimization can be accomplished by adjusting the gate aspect ratio of the biasing transistor for a specific optical input. For 0.5-mW optical input power and a 25-\( \mu \)m diameter detector, response times of 2.2, 1.1, and 0.8 ns can be achieved with typical 2, 1, and 0.5-\( \mu \)m technologies respectively. These times can be further reduced by increasing the optical power or reducing the detector size. The circuit can also be easily extended with a low-gain stage for more fan-out or higher speed operation. The presented circuit is compatible with standard IC processing and the optimum design is relatively simple.
REFERENCES