Message from the General Chair

Welcome to Santa Clara and the 25th Annual Symposium on High-Performance Interconnects, generously hosted by Ericsson. This forum brings together researchers, developers, and users of state-of-the-art interconnection networks of all scales, ranging from multi-core on-chip interconnects to those within systems, clusters, and data centers. We are honored to present to you an exciting three-day program, filled with high-profile keynote presentations, in-depth technical sessions reporting on cutting-edge research, vivacious panel discussions, and enlightening tutorials.

Many thanks to Ryan Grant and Jitu (Jitendra) Padhye for serving as technical program co-chairs. They organized and led the technical program committee, which reviewed the papers to appear in these proceedings, to select a collection of high-quality submissions covering a wide spectrum of topics, ranging from on-chip communication, to large scale networking, to datacenter and HPC fabric management. We are also pleased to include several invited talks from experts from Ericsson, HP, Microsoft and Google.

We are grateful to have outstanding keynote speakers: Chuanxiong Guo from Microsoft Research will describe the newest advances in “RDMA deployments: From Cloud Computing to Machine Learning”, and Nandita Dukkipati from Google will reveal the innovations behind the “Performance Isolation for Highly Efficient Shared Infrastructure Services”. David Allan from Ericsson will discuss the new challenges brought by “Information Transfer in the Era of 5G”, and Paolo Faraboschi from Hewlett Packard Labs will discuss the roadmap for “Communication at the Speed of Memory”.

We are particularly thankful to Dan Pitt and Méral Shirazipour for organizing a dynamic panel discussion on Ethernet vs. HPC fabrics, raising the question “Can the hyperscale Ethernet data center handle all workloads”. We express our gratitude for the participation of all panelists: Yogesh Bhatt from Ericsson, Dave Cohen from Intel, Pete Fiacco from GigaIO, Bhithika Khargharia former Extreme Networks, Dave Meyer from Brocade and Ying Zhang from Facebook, and to Roy Chua from SDxCentral for serving as a panel moderator.

The Monday tutorials provide a variety of topics of interest to the Hot Interconnects community. We thank James Dinan and Khaled Hamidouche for selecting and organizing five high-quality tutorials on hot topics of high-performance and data center networking, delivered by leading experts: “Exploiting High-Performance Interconnects to Accelerate Big Data Processing with Hadoop, Spark, Memcached, and gRPC/TensorFlow” by D. K. Panda, X. Lu, Ohio State University; “High Performance Distributed Deep Learning for Dummies” by D. K. Panda, A. A. Awan, and H. Subramoni, Ohio State University; “Designing and Developing Performance Portable Network Codes” by Pavel Shamis, ARM; Yossi Itigin, Mellanox Technologies; “Developing to Open Fabrics Interfaces libfabric” by Sean Hefty, Intel, James Swaro, Cray; and “The TraceR/CODES Framework for Application Simulations on HPC Networks” by Nikhil Jain, LLNL; Misbah Mubarak, ANL.
The HOTI committee veterans, Madeleine Glick, Xinyu Que have provided their invaluable contribution to Hot Interconnects, serving as finance co-chairs, working effectively with IEEE during the budget approval. Similarly, Krnee Deemark has put tremendous effort into the success of the event through her role as local arrangements chair. We thank them heartily for their enthusiasm, commitment, and leadership.

Thanks to Luca Valcarenghi for flawlessly handling the proceedings, and Lisa O’Conner and Patrick Kellenberger of the IEEE Computer Society for working with us on a very tight schedule. We appreciate the help of Natalia Berezneva as webmaster, building a marvelous web site that can be visited on-line at http://www.hoti.org. We thank Torsten Hoefler for serving as media-relations co-chairs, and Songkrant Muneenaem as registration chair.

Hot Interconnects would be much less successful without the financial help of our sponsors. We deeply appreciate the generous support of our official sponsor the IEEE Computer Society and the Technical Committee on Microcomputers and Microprocessors, and of our industrial patrons that are listed on the webpage and in the conference program and Raj Channa for coordinating the sponsoring program. Finally, we would like to extend our gratitude to Ericsson for graciously hosting the conference in their state-of-the-art campus in Santa Clara, in the heart of Silicon Valley.

Ada Gavrilovska, Georgia Tech
Eitan Zahavi, Mellanox
Elisabetta Romano, Ericsson
HOTI 2017, General Chairs