1.0 Introduction

Embedded processors are being used in numerous applications like automotive systems, hand-held devices, set-top boxes, network routing, wireless communications etc. Due to the nature of these applications, processors must have low power requirements, low price, small memory and yet high computational power. There is a significant research in the area of processor architectures for embedded applications both in industry and academia. In current market place one can find a wide variety of processors in terms of

- size (4, 8, 16, 32 and 64 bit) and
- architecture (RISC, CISC, Super-Scalar, VLIW, parallel) and
- supported peripherals

Traditionally these processors were tuned for a specific application like audio, video or graphics and had application specific instruction set architectures and were programmed in assembly languages. The complexity of developing, maintaining and time to market considerations of products based on these processors is causing a significant effort being devoted to the task of easing software development task for these processors. A primary focus in this endeavor is the development of software tools like compilers, assemblers, debuggers, profilers and simulators. There are significant challenges facing software tool developers in dealing with compiler optimizations, performance prediction, high speed cycle accurate simulations, programming paradigms to take advantage of architectural features. All these issues are made more complicated by the system on chip solutions where there are multiple heterogeneous cores on a single chip. This track is a forum for researchers to present their ideas about these issues in software tools for embedded systems.

2.0 About the Minitrack

This minitrack received 15 abstracts in the initial call for papers. Of these 12 full manuscripts were submitted in the area of architectures, compilers, programming paradigms and formal verification. Each paper was reviewed by at least four (4) referees for content, quality, accuracy and relevancy to minitrack. Five (5) papers were finally selected.

Two of the selected papers were in embedded processor architectures. In the paper titled ‘An infrastructure for Designing Custom Embedded Counterflow Pipelines’, the authors propose and evaluate an extension to the counterflow pipeline organization, which they already developed in earlier work, called wide counterflow pipeline and specify a method of automatically generating such pipelines. In the paper titled ‘A Re-configurable Processor for a Petri Net Simulation’, the authors describe Achilles, a configurable and scalable programmable FPGA based processor/system and evaluate programming petri-net simulation software on this system.

Two papers in the compilation area are selected for presentation. In the paper titled ‘A new approach to DSP intrinsic functions’, the authors describe an alternative approach to implementing intrinsics in ANSI-C compilers targeted to DSPs which achieves better performance and is less architecture dependent than other approaches. In the paper titled ‘Reverse compilation for Digital Signal Processors: a working example’, the authors describe the development and evaluation of a decompiler that translates AD 21xx assembly language to ANSI-C.

One paper was selected in the area of formal verification. In the paper titled ‘The Production Cell: An Exercise in the Formal Verification of a UML Model’, the authors extend UML model to analyze the behavior of the Production Cell, which is a well-known case study in the formal methods community. They describe a verification tool, called vUML, which translates a collection of UML state chart diagrams into a Promela model, which is then fed into the SPIN model checker for analysis.

3.0 Conclusion and Acknowledgment

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