Modelling and Exploration Environment for Application Specific Multiprocessor Systems

Ismail Assayad
Verimag, Grenoble, France
ismail.assayad@imag.fr

Sergio Yovine
Verimag, Grenoble, France
sergio.yovine@imag.fr

Abstract—We present a tool-assisted platform-based design flow for embedded multiprocessor applications. The methodology relies on (1) a formal language which provides constructs to specify the platform-independent behavior of an application using an abstract execution model, and to describe the micro-architecture components of the hardware architecture, together with its compilation chain JAHUEL [1], and (2) a component-based meta-model for joint software and hardware performance modelling and analysis, together with its simulation tool P-W ARE [2], which provides fast, precise and scalable platform-level simulations. JAHUEL and P-W ARE have been successfully used for the design of industrial multimedia and packet-forwarding embedded software on application-specific multiprocessor architectures.

Keywords: Multiprocessor Embedded Systems, Architecture Exploration, Software/Hardware Analysis.

I. INTRODUCTION

The rapidly increasing performance requirements of embedded applications, such as HDTV and high-speed networking, motivated the production of customized, network-centric, multi-processor hardware platforms, e.g., Intel IXPXX NP and Philips Wasabi/Cake, composed of multiple heterogeneous, multi-threaded processors, which communicate through sophisticated interconnects. To exploit the benefits introduced by these application-oriented architectures, there is a need to develop a design, analysis and implementation flow providing integrated, rather than separate, software and hardware modelling and simulation. The main challenge is to provide methodologies and tools capable of supporting accurate, but fast, performance analysis for dimensioning the hardware platform and mapping of software.

To this end, we have developed a platform-based design [3] framework composed of a code-generation tool, JAHUEL [1], and a simulation tool, P-W ARE [2].

JAHUEL is based on formal language which provides (1) platform-independent constructs for parallel software programming application using an abstract execution model, and (2) semantic and syntactic support for architecture-dependent code-generation via program transformations. P-W ARE relies on a formal component-oriented meta-model for cleanly composing hardware and software sub-systems without interfacing wrappers.

In the context of an academic-industrial cooperation, current work in progress aims to develop a design flow which starts from a high-level modelling of application software and hardware, all the way down to the concrete implementation and mapping (currently manual), while going through the synthesis of an application-specific software scheduler [4] (currently manual), the analysis of software/hardware joint performance simulation, and the generation of executable code.

II. METHODOLOGY

Setting up a system with this framework is operated as follows (figure 1). First of all, JAHUEL is used to define the models of the application and the architecture. The application is the software (eg., a video encoder) and its environment (eg., camera and display devices), while the architecture is the underlying execution hardware (eg., processors, buses, caches, etc.). The application model only takes into account environment execution times and periodic activations, and software and environment interactions due to data and control dependencies. That is, the model abstracts away from hardware-dependent issues, such as conflicts between software and environment communication due to concurrent bus and memory accesses, and, as a consequence of this abstraction, software execution and communication times are treated as unknown parameters.

Then, the step “constraint synthesis” derives a scheduler of this application and a constraint on the parameters which must be satisfied at runtime, by any parallel mapping of software which will be defined later. After that, we look for software implementations, i.e., mappings on processors, which must satisfy the latter constraint. This is done by considering several classes of parallel implementations (eg., data parallel, task parallel and hybrid implementations).

Software components corresponding to each of these implementations are generated, in addition to the hardware ones and their bindings, as input to P-W ARE.

If performance objectives are met, JAHUEL synthesizes the executable code of software.

III. A SIMPLE PRODUCER/CONSUMER SYSTEM

The software is composed of two elements: a producer (Writer) and a consumer (User). The snippet code below depicts the FXML model. The producer is an infinite loop writing a variable x and the consumer is an infinite loop reading it. Data dependencies, time properties and constraints are also specified in the model by the content of dep-list, execution-time and period elements, respectively. Writer and User are concurrent and are thus put inside a pnode-sum element, used to specify task parallelism.

```xml
<SW Model>
  <Constraints Synthesis>
    <SW Model HW Model>
      <Mapping of SW over HW>
        <SW Model>
          <SW Implementation/SW+HW Components generation>
            <P-W ARE Components>
              <P-W ARE Simulation>
  </SW Model HW Model>
</SW Model>
```

Fig. 1. Analysis methodology

1. `<pnode-sum>` ...
2. `<dep-list> ... </dep-list>`
3. `<body>`
4. `|-- Writer -->`
5. `<while>`
6. `<label>Writer</label>`
7. `<condition>`
8. `<b-exp>`
9. `<boolean default-value='true'/>`
10. `<b-exp>`
11. `</condition>`
12. `<period>`
13. `<time>30</time>`
14. `<time-unit>us</time-unit>`
15. `</period>`
16. `<body>`
17. `...`
18. `<source-code>`
19. `function write();`

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The hardware is composed of two processors, accessing the off-chip memory through two DMAs and one data bus. Hardware components may be connected to one or several target components. The caller can send transactions requests (TR) (eg. read/write) to the recipient through its output ports. These bindings are specified in the snippet code below by elements qinput and qoutput, for one-to-one or one-to-n ports bindings, respectively.

```xml
<Bus>
  <-- CHANNEL definition -->
  <id>1</id>
  <qin>RBUS</qin>
  <qoutput>DMA1</qoutput>
  <number>1</number>
  ... 
  <clock-port>CLK</clock-port>
</Bus>
```

A. From JAHUEL to P-WARE

To produce P-WARE components code for the Producuer/Consumer example above, JAHUEL was configured to operate the following sequence of transformations:

1. Components code generation
2. P-Ware SW and HW component library
3. P-Ware main entry

The componentization step encapsulates the FXML nodes into software component objects. Current possible componentizations consist of mapping each leaf to a P-WARE software component, where a leaf is a node which has no pnode-sequence or pnode-num as a descendent in its syntax tree. Componentization may also be derived using components names given by designer in a mapping attribute attached to the software nodes.

The synchronization step implements the FXML pnodes dependencies and timing constraints. It consists of adding the definition of the scheduler block for each component in the FXML model. This is done by indicating for each pnode its role in a dependency (senders or recipients), the dependency pattern (eg. the recipient must wait all senders), the number of senders and the number of recipients and timing constraints.

Finally, components code is generated for P-WARE by applying a set of code generation templates (stylesheets), where a template is a pair composed of a pnode name in the software syntax tree, and a rule to apply when this pnode is matched.

Figures below depict bindings of the generated Writer/User system, and as an example, the CHANNEL component model, and the MEMORY component model, respectively.

B. Performance monitoring

Given a set of hardware and software components, automated behavior monitoring is achieved by P-WARE meta-model integrated performance observers.

As an example, figure below shows the disparity of tasks synchronization times provided by the tool, for a task-parallel implementation of a part II MPEG-4 implementation using the 16 range based hierarchical motion estimation algorithm, H16, on the Philips Cake architecture including up to 8 processors.

IV. CONCLUSION

JAHUEL/P-WARE is a flexible and extensible tool-suite which provides a platform-based design flow for multiprocessor embedded systems. Our framework supports modelling, code-generation and joint software/ hardware performance simulation which enables fast and precise exploration of different system configurations, both at software and hardware levels, in order to find one that meets QoS requirements. In this paper, we gave an overview of JAHUEL modelling and exploration environment on the top of P-WARE simulation tool.

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REFERENCES


