A Design for Concurrent Error Detections in FPLAs

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Abstract

In this paper, a combined design of four concurrent error detection (CED) schemes — the alternating logic scheme, duplication the on-set scheme, duplication the off-set scheme, and the parity checking scheme, is proposed to be argumented into the field programmable logic arrays (FPLAs) which inherently has unutilized elements. One of the four CED scheme can be implemented by the proposed circuit and the unutilized elements with the constraint that the unused elements are enough to be programmed as parts of test logic.

1. Introduction

Field Programmable Logic Arrays (FPLAs) [1–5] allow the synthesis of complex logic functions by user in the field. In other words, user can edit, even repeatly program, the desired functions in the field with the advantages of shorter development cycles, design flexibility, and quick recovery from design error.

As shown in Figure 1 [1], an FPLA usually has fix number of inputs, outputs and product lines (in this case, 16 inputs, 48 product lines, and 8 outputs). When implementing the desired functions, the required space may be relatively small, i.e., large parts of the FPLA may be wasted.

The basic concept of this paper is that, in stead of just wasting, these unutilized space, with the proposed design, can be implemented as testing logic for concurrent error detection (CED). The assumption of this paper is that the unused space is enough to implement one of the CED schemes discussed latter. If the space is not enough, then partial CED scheme can be studied in the future research direction, which will not be discussed in this paper.

This paper is organized as follows. Each proposed design of four CED schemes is presented and explained in Section 2. Followed by the simulation of the major part of the proposed design in Section 3. Finally, a conclusion is remarked in Section 4.

2. Proposed Design

In this paper, a design for four CED schemes — the alternating logic (AL) scheme [6,7], duplication the on-set scheme (DON) [7], duplication the off-set scheme (DOFF) [7], and the parity checking scheme (PC) [7], is proposed to detect faults at the run-time. One of the four CED scheme can be implemented by the proposed circuit and the unutilized elements.

As shown in Figures 2 and 3, the proposed design requires three extra input pins, four extra output pins, and some testing circuits. Signals ALTest and PrCl are used for AL scheme and PC scheme,

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respectively; while signal Dtest is applied for both DON and DOFF scheme.

A totally self-checker (TSC) [8] is argumented to show the test result of AL, DON, and DOFF schemes. The inputs of TSC should be in pair with complemented values, and the results is shown by two complemented error indicator T1 and T2, if no error is occurred.

For PC scheme, two exclusive-OR gate chains are argumented in the output lines and product lines with two extra output pins PP (product parity) and OP (output parity), respectively. The output line parity checking chain, illustrated in Figure 3, is obtained by setting control signal PrCl = 1, and Dtest =0. For AL scheme, a exclusive-OR gate array is added in the inputs to complement the input signals.

The control signals for each CED scheme is listed in Table 1. The test result is observed from extra pins PP and OP for PC scheme, and T1 and T2 for the rest three schemes.

To explain the AL scheme and PC scheme, an example with function F_1= AB+BC+AC and F_2= A'C+B will be demonstrated in both schemes, where A' means the complement of variable A.

2.1 Alternating Scheme

To apply alternating scheme for concurrent error detection, there are two constraints. First, being one of the time redundancy techniques [7], the AL scheme requires recomputation, and then compares both results. Therefore, the AL scheme can be applied only if the timing is allowed to perform recomputation. The result of first computation is stored in flip-flops for latter comparison.

Secondly, the AL scheme can only applied to test a function f(x) which has the property of f '(x_1, x_2, ..., x_n) = f ((x_1', x_2', ..., x_n'). This property is called *self-dual* [6,7].

To apply AL scheme to FPLA for CED design, the output functions must be modified to be self-dual, if originally there are not. This work can be done, if necessary, by adding at most one extra inputs [6] and several unused product lines. The number of extra product lines may be significantly large. However, it is assumed that the unused space in the FPLA is enough for implementing one of four proposed CED schemes.

The reconfiguration of AL scheme is shown in Figure 4. In the first computation, control signal ALTest is 0, and result is stored in flip-flops. In the second computation, input signals are complemented by the exclusive-or gate array of the inputs of FPLA by setting ALTest = 1. Both results are then fed into a TSC. If both outputs are complemented, the no fault is detected, i.e., error indicators T1 =T2'. Otherwise, T1=T2 indicates at least a fault is detected.

In the example, F_1 is self-dual but F_2. Therefore, an extra input H is added to change F_2 (= BC+H'B+A'B+H'A'C) to be self-dual as shown in Figure 5. Thus, two extra product lines and one extra input line are required.

2.2 Duplication of the on set and off schemes

The simplest testing concept is to duplicate the original function with the same amount of hardware. Then compare both outputs with each other. Both outputs should be equal, if no fault is presented in the circuit. This scheme, called *DON* scheme, just copies original circuit, and the area overhead is, therefore, 100%.

Similar to the DON scheme, the *DOFF* scheme implements the complement logic of original function in the unsed space, such that both outputs are complemented.

The area overhead for implementing DON and DOFF schemes can be reduced if the CAD tools for PLA minimization, such as *playground[9], espresso[10]* are used.

As shown in Figure 6, control line Dtest is used to make complemented signals in pair which are fed into TSC, i.e., Dtest=1 (=0) for DON (DOFF) scheme. If error indicators T1 = T2', then no error is detected as discussed before.

2.3 Parity Checking Scheme

If the inputs can simultaneously enable odd or even number of product lines and outputs, then the PS scheme can be applied. The FPLA is argumented by parity checking chains in both product lines and output lines as illustrated in Figure 7. Faults are detected if the parity is changed form odd (even) to even (odd).

As shown in Figure 8, for the odd parity of product lines, product terms B'C'and AB are argumented; while for odd parity of output lines, an extra output F_3 = B'C'+BC+AB is added. The number listed in each minterm of Figure 8 is the number of product lines or output lines activated. Two extra product lines, P6 and P7, are required for this example as shown in Figure 9. Note that to enable odd number of product lines, two product lines are equal (P7=AB = P1).

3. Simulation

To verify the proposed design and for simplicity, the proposed checking circuit with only two outputs of the FPLA is simulated by *Micro-logic II* [11]. The gate level diagram and the result of simulation are shown in Figures 10 and 11, respectively. In Figure 10, two FPLA outputs OUT1 and OUT2 are fed as inputs of the checking circuit; while the results are indicated by outputs OP (for PC scheme) , T1, and T2 (for the rest three schemes). Signal PRCL, DTEST, ALTEST are control inputs for the checking circuit.

The results of the simulation, as illustrated in Figure 11, is explained as follows. The DON scheme (ALTest=0, PrCl=0, and Dtest=1) is tested during time interval t_1, and t_2 with a correct result and an incorrect one in sequence. The fault is detected from observing TSC outputs, i.e., T1 = T2 as illustrated at t_2. Similarly, the DOFF scheme (ALTest=0, PrCl=0, and Dtest=0) is verified at t_3 and t_4. The PC scheme (ALTest=0, PrCl=1, and Dtest=0) is simulated at t_5 and t_6 with odd and even parities, respectively, as indicated at outputs OP. The last CED scheme, AL scheme, is verified during t_7 to t_{10}. Recall that each AL scheme requires two time intervals for recomputing and then comparing. The results of the comparisons are evaluated at the falling edge of the second clock as shown in t_8 and t_{10}.

4. Conclusions

In this paper, a combined design of four concurrent error detection schemes — the alternating logic scheme, duplication the on-set scheme, duplication the off-set scheme, and the parity checking scheme, is proposed to be argumented into the field programmable logic arrays which inherently has unutilized elements. One of the four CED scheme can be implemented by the proposed circuit and the unutilized elements with the constraint that the unused elements are enough to be programmed as parts of test logic.

However, if the unused space is not enough for implementing any one of the four CED schemes, in the future research area, a partial CED scheme of the four types can be studied to obtain the highest fault coverage. In other words, if the probability of each fault model is given, how to utilize the limited space in order to get maximum testability is the future research direction.

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Figure 1 The structure of a Field Programmable Logic Array [1].

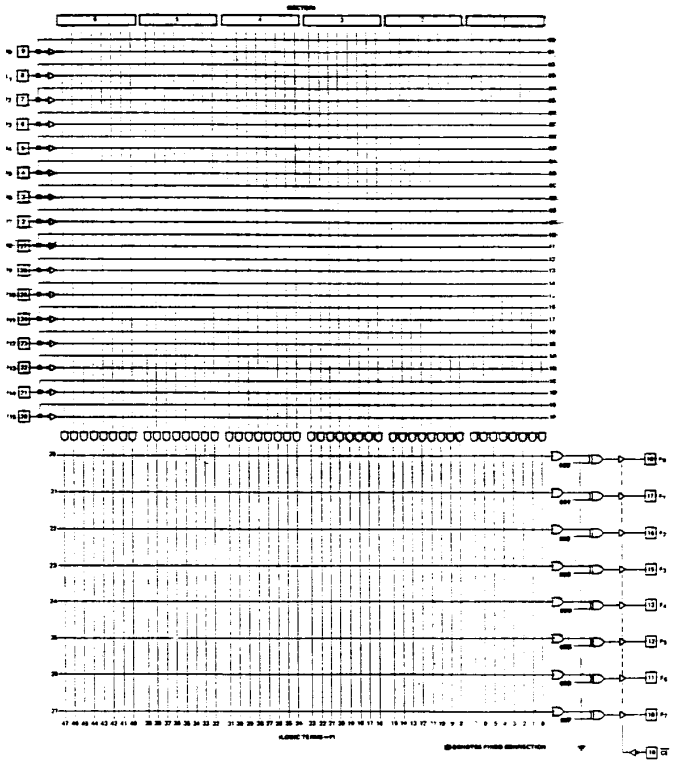

Figure 2 Block diagram of Proposed Design

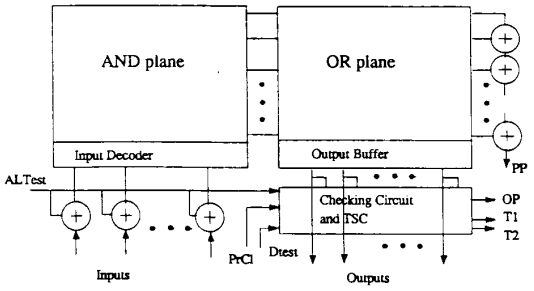

Figure 3 The proposed checking circuit at the outputs of the FPLA.

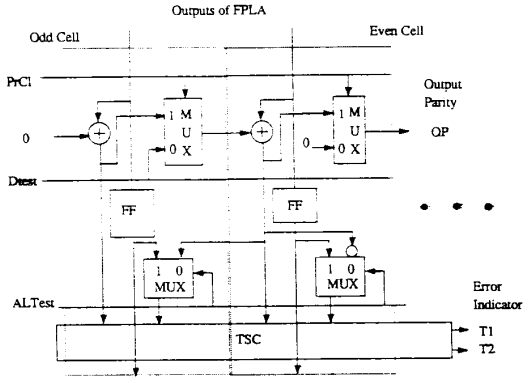

Figure 4 The reconfiguration for AL scheme

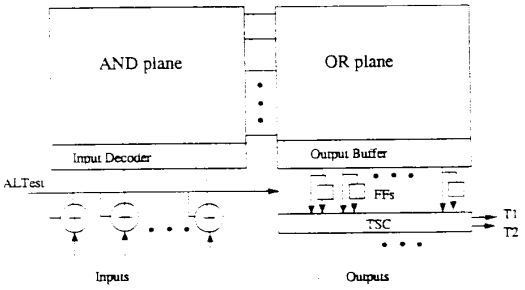

Figure 5 An example to explain AL scheme

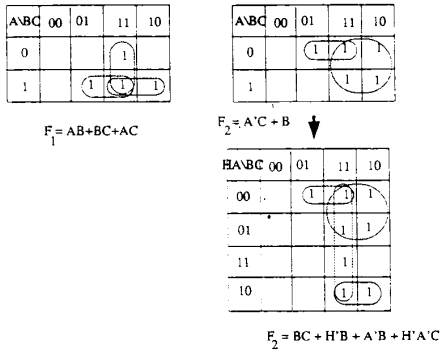

Table 1 Control signals for the corresponding CED scheme.

Scheme \ I/O	ALTest	Dtest	PrCl	T1,T2	PP,OP
AL	0 then 1	0	0	T1=T2'	don't care
DON	0	1	0	T1=T2'	don't care
DOFF	0	0	0	T1=T2'	don't care
PC	0	0	1	don't care	Used

Figure 6 The reconfiguration of DON and DOFF schemes.

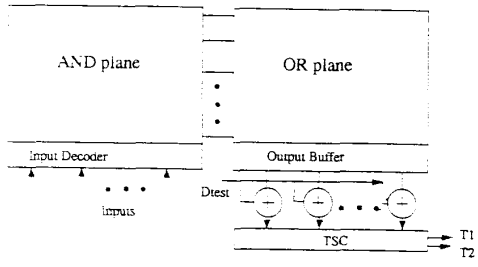

Figure 7 The reconfiguration of PC scheme.

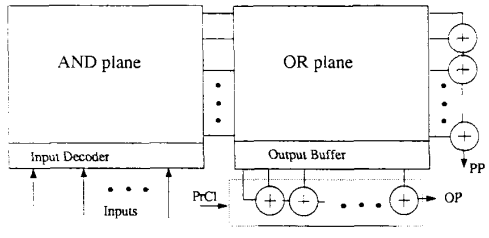

Figure 8 An example to explain PC scheme

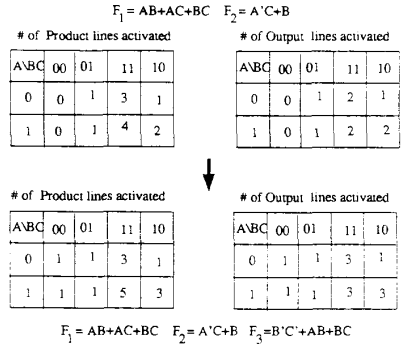

Figure 9 The reconfiguration of the example for PC scheme.

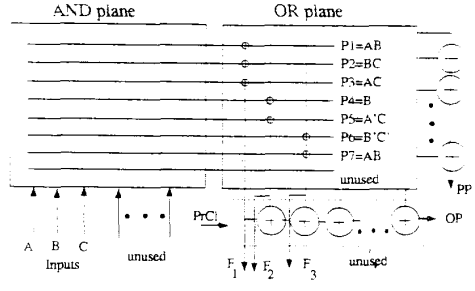

Figure 10 Gate level diagram for simulating major part of the proposed circuit.

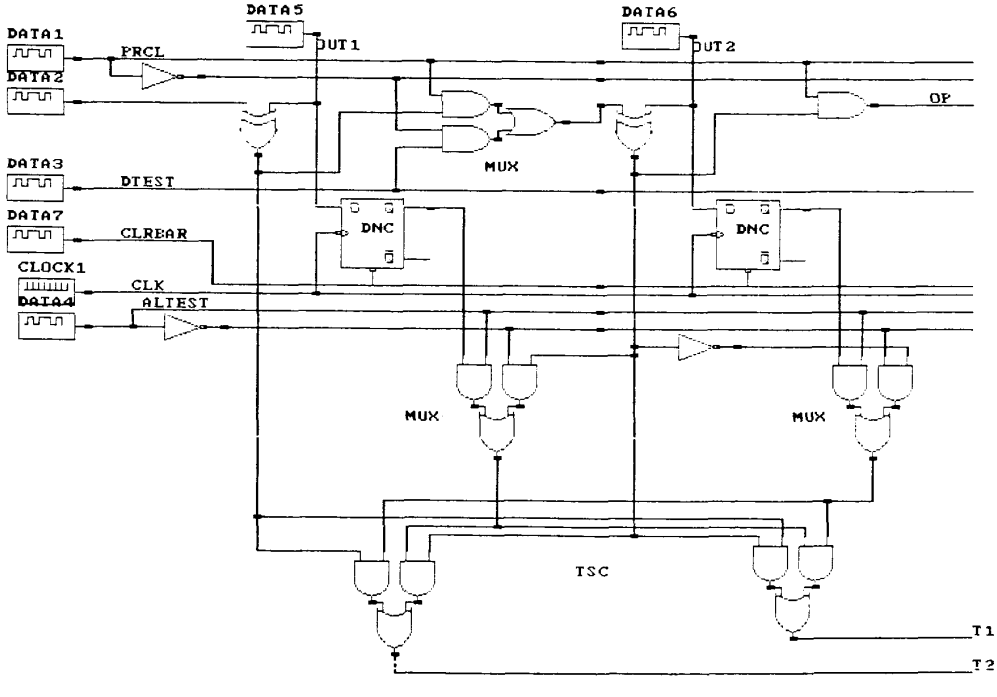

Figure 11 Simulation results