A Signed Hypergraph Model of Constrained Via Minimization

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Abstract

We propose a use of the notion of hypergraphs to describe the general constrained via minimization (CVM) problem. We show that the formulation of the general CVM by means of hypergraphs turns out to be surprisingly simple and general. In the case of two-layer routing, a signed hypergraph model is introduced. On the basis of this model, we develop a fast (linear-time) heuristic and obtain promising results; we also present two methods of modeling multi-way splits by graphs, producing better results than all the previous methods.

1 Introduction

Constrained Via Minimization (CVM) arises in Integrated Circuit (IC) layout and in Printed Circuit Board (PCB) design. In this paper, we consider the mathematical modeling aspect of the CVM problem. For the sake of simplicity, we will study the problem in the context of IC chip layout; the results are directly applicable to PCB design. (We hope that, with certain modifications, the results are also applicable to the multichip modules (MCM) technology.)

A *circuit* consists of a set of *modules*, each being a connected region in the plane, and a set of *nets*, each of which specifies a subset of points located on the boundary of modules, called *terminals*. Circuit input and output pins can be viewed as special modules that provide one terminal each module.

A major aspect of Very Large Scale Integrated (VLSI) circuit design is automatic generation of physical layout. It involves *placement*, i.e., finding a placement of the modules in the plane, and *routing*, i.e., interconnecting the terminals as specified by the nets. The routing of signal nets is usually accomplished by means of vertical and horizontal *wire segments*. We assume that there are l-layers. Wire segments of the different signal nets that cross each other, or if placed on the same layer will overlap (as restricted by physical design rules), should be assigned to the different layers. A *via* is used to connect the wire segments of the same signal net assigned to the different layers. Vias not only decrease the reliability, yield, and performance of the circuit, but also increase the manufacture costs. Therefore, it is highly desirable to minimize the number of vias used.

One approach to via minimization is to route signal nets with the primary objective to minimize the number of vias. This is the *topological routing* methodology, where only the positions of terminals are specified and the task is to determine the topology of signal nets such that the number of vias is minimized. Hence, it is also known as *topological via minimization* (TVM). Some recent effort in topological routing has produced very promising results that are comparable to routings obtained from conventional routing methodologies in terms of area and wire length[20]. However, TVM is still in the research progress, and most current topological routings achieve the goal of via minimization at the expense of irregular layout wiring, longer total wire length, and even worse circuit performance.

A more practical approach is assuming that the routing of signal nets has been done in a manner to minimize the area and total wire length, only layer assignment of wire segments is to be determined so as to minimize the number of vias. Since the geometry of each wire segment is fixed, it is *constrained via minimization* (CVM), as opposed to the case of topological via minimization, which is also called unconstrained via minimization.

CVM is more relevant than TVM, not only in the sense of practicality, but also due to the following two reasons. First, TVM can be done by means of CVM[22], and TVM may contain a step of CVM[10]. Second, it is possible and desirable to use CVM to improve the results given by TVM, because of the simplicity of TVM models and the approximation of TVM algorithms. Therefore, we concentrate on the CVM problem in this paper.

This paper is structured as follows: In Section 2, we present a general mathematical model, called the black-white hypergraph, to capture the general CVM problem of l-layers. We study the feasibility problem of layer assignment in Section 3. In Section 4, we show that the CVM of two-layer routing can be significantly simplified by using

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the notion of signed hypergraph. We describe two types of constraints and show how to use them to model various practical constraints in Section 5. Section 6 summarize some results obtained by means of the signed hypergraph model. A brief review of some related work is given in Section 7. Section 8 concludes the paper.

2 Black-White Hypergraph Representation of Partial Routings for CVM

It is assumed that the placement of circuit modules and the routing of signal nets have already taken place and the resulting routing is represented by a fixed set of interconnecting wire segments. Any two wire segments that cross each other, overlay, or otherwise violate physical design rules if placed on the same layer, are called *conflicting*. A *cross point* is used to represent the conflicting of two wire segments. A *junction* is a point other than terminal where two or more wire segments meet and are electrically connected. A junction is also called *via candidate* or *potential via* in the literature, since we may always place vias at the junctions. The number of wire segments that meet at a particular junction will be referred to as the *junction degree*. As a special case, if we choose to place a via in a wire segment, then the chosen wire segment is broken into two wire segments connected by a junction with degree 2. Junctions with degree higher than 2 are traditionally called *splits*. A layer assignment is *feasible* if no two conflicting wire segments are assigned the same layer.

We start with a *partial routing*, denoted by R, which consist of a set of junctions and a collection of wire segments implementing all the signal nets without specifying which layer each wire segment belongs to. A *complete routing* consists of a set of wire segments, a set of vias, and a valid layer assignment which correctly realizes the interconnection requirements specified by the netlist. Note that a partial routing may result from some routing methodologies where the actual layer assignment is to be determined, for examples, topological routing[10, 22] or knock-knee routing[12]. It may be a complete routing obtained from some automatic CAD tools. In the latter case, the given layer assignment may be used in iterative improvement-based algorithms as an initial solution to the CVM problem, however, we simply ignore such information in the modeling phase.

Example 1 Consider Fig. 1. It has five two-terminal signal nets:

- N_a: wire segment $a1$,
- N_b: wire segments $b1$, $b2$, and $b3$,

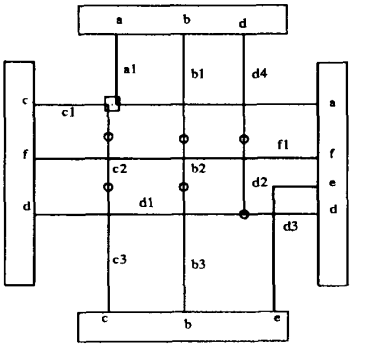

Figure 1: A partial routing R_1

- N_c: wire segments $c1$, $c2$, and $c3$,
- N_e: wire segment $e1$,
- N_f: wire segment $f1$,

and one three-terminal net:

- N_d: wire segments $d1$, $d2$, $d3$ and $d4$.

There are eight cross points, one knock-knee point marked by a square, and six junctions marked by $\circ$. S knock-knee point can be treated exactly in the same way as a cross point. □

The routing shown in Fig. 1, as often used in the CVM research, is already a symbolic representation of the actual physical routing. However, it can be further abstracted. The primary objects here are a set of wire segments, which are related either by junctions or by crossing points. Therefore, it is natural to use a graph representation, where wire segments are represented by vertices, junctions and crossing points by edges. Junctions and crossing points represent two different relations among vertices; we distinguish them by using two types of edges, called the *black* and *white* edges. A junction may connect more than two wire segments (c.f. split), hence, the corresponding edge may connect more than two vertices, and the representation is a hypergraph. More formally, the black-white hypergraph representation is defined as below.

Definition 1 *Consider a partial routing R. $\mathcal{H}(R) = (V, C \cup E)$, is the* **black-white hypergraph** *of R, where vertex $v_i \in V$ represents a wire segment of R, white edge $c_i \in C$ corresponds to a crossing point of R, and black edge $e_i \in E$ corresponds to a junction of R.*

The black-white hypergraph for partial routing R_1 in Fig. 1 is shown in Fig. 2, where the white edges are represented by dash curves and the black edges are represented by solid curves. We choose to represent an edge by an open curve with multiple end-points, instead of circles used in the conventional hypergraph theory[2].

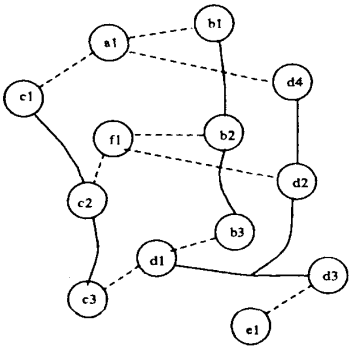

Figure 2: Black-white hypergraph $\mathcal{H}_1$ of routing R_1

The vertices connected to an edge is said to be the edge's vertices. The number of vertices connected to an edge is referred to as the *edge degree*, denoted by $|c_i|$ (or $|e_i|$). For two-layer physical routings, $|c_i|$ is usually equal to two. However, in general, it is possible that $|c_i|$ is also larger than two. If all the edge degrees are equal to two, then $\mathcal{H}$ is a *black-white graph*.

The notation of black-white hypergraph captures exactly how wire segments connect together to form a signal net and how wire segments conflict with each other, both of which are determined uniquely by the relative geometric information of a given partial routing. As a consequence, the CVM problem can be stated more abstractly in terms of the black-white hypergraph. To facilitate such an abstraction, we further introduce some graph-theoretic concepts. A l-way *partition* of V is a separation of V into l disjoint subsets, called *groups*. A black edge is said to be *balanced* by a partition if all its vertices belong to one group; a white edge is said to be *balanced* by a partition if all its vertices belong to different groups, i.e., none of any two vertices of the white edge belong to the same group. Intuitively, we may color all the vertices belonging to a group by black, and also color the curves connecting "black" vertices by black. Initially all the curves are white. Therefore, a black edge is balanced by a partion if it is colored completely by black and a white edge is balanced by a partition if it remains completely white. An unbalanced black edge means that there is a via required at the corresponding junction.

Proposition 1 *Given a partial routing R, let its black-white hypergraph to be $\mathcal{H}(R) = (V, C \cup E)$, the CVM problem for R is equivalent to finding a partition of V into l groups such that (1) all white edges are balanced, and (2) the number of unbalanced black edges is minimized.*

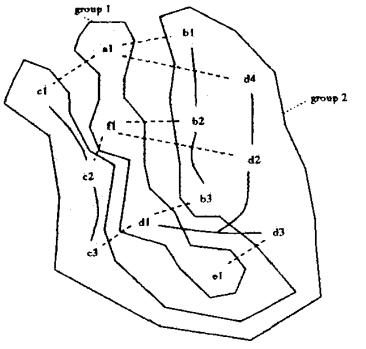

Figure 3: A two-way partition of $\mathcal{H}_1$

The satisfaction of condition (1) is a matter of whether all signal nets can be wired using l layers under the the given set of potential vias. This is the *feasibility problem* of l-layer assignment for a partial routing.

3 Feasibility of Layer Assignment

In this section, we study the feasibility problem of layer assignment. It is a restricted version of the wirability problem, since the geometric positions of wire segments are fixed. We first state a general result that relates the feasibility of layer assignment to the colorability of a graph. We then present a Boolean satisfiability formulation.

Feasibility via graph colorability

If the feasibility of layer assignment is concerned, only the white edges in the black-white hypergraph are of interest. To simplify our discussion, we introduce the following concept.

Definition 2 *Consider a partial routing R. $G(R) = (V, C)$ is the constraint graph of R, where vertex $v_i \in V$ represents a wire segment of R and edge $c_i \in C$ corresponds to a crossing point of R.*

The constraint graph G of R is its corresponding black-white hypergraph $\mathcal{H}$ without black edges. The constraint graph G_1 for routing R_1 is shown in Fig. 4.

Given a graph G, consider to mark each vertex by one color. If all the vertices in a graph can be marked by l colors such that no two adjacent vertices have the same color, then G is said to be l-colorable.

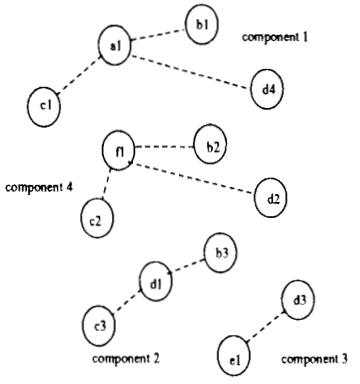

Figure 4: Constraint graph of routing R_1

Proposition 2 *The CVM problem of a partial routing R has a feasible l-layer assignment solution if and only if the corresponding constraint graph $G(R)$ is l-colorable.*

Proof.

Necessity: If the constraint graph G is non-colorable with l colors, that means, there is at least one edge in G connecting two vertices with the same color. Thus there exist at least two conflicting wire segments assigned to the same layer. So we cannot have a feasible layer assignment to the CVM problem.

Sufficiency: If the constraint graph is l-colorable, any two adjacent vertices connecting by edges in G are assigned different colors. This means that all conflicting wire segments are assigned to different layers. Vias will be used to connect wire segments belonging to the same net but assigned to different layers. So we have a feasible layer assignment. □

So far, we assumed that all the edges in a constraint graph connect only two vertices. In general, it is not true, since several wire segments may mutually conflict with each other.

Remark 1 *The CVM is l-layer wirable, only if there are no edges in its constraint graph with degree greater than $l-1$.*

In graph theory, a *clique* is a complete subgraph, i.e., there exists an edge between every two vertices. The following remark states that we can always concentrate on the constraint graph with edges of degree two.

Remark 2 *The constraint graph is equivalent to the one by replacing all the edges with degree larger than two by their corresponding cliques.*

Feasibility via Boolean satisfiability

The graph l-colorability problem is NP-complete. Instead of designing heuristics for feasibility checking, we describe a Boolean satisfiability formulation. The motivation is due to the fact that efficient checkers of Boolean satisfiability are available from recent research effort in Boolean logic minimization and have demonstrated promising performance in solving some practical layout problems[8].

For the sake of simplicity, we assume that $l = 3$. We need $p = \lceil \log_2(l) \rceil = \lceil \log_2(3) \rceil = 2$ Boolean variables to encode all the l-colors. For $p = 2$ Boolean variables, there are $2^p = 4$ distinct combinations of 0/1 assignments. Here, they are 00, 01, 10, and 11. We may arbitrarily choose l distinct combinations as an encoding to l-colors. Without loss of generality, we assume that we use 01, 10 and 11 to represent three colors.

Associated with each vertex, $v_i \in V$, we assign $p = 2$ Boolean variables, namely x_{i1}, x_{i2}. In order to have a 0/1 assignment to $x_{i1}x_{i2}$ to be a valid color, $x_{i1}x_{i2}$ cannot be equal to 00. Therefore, we have the following constraint associated with each vertex.

$$\overline{x}_{i1}\overline{x}_{i2} = 0. \tag{1}$$

In general, there exist $2^p - l$ such constraints for each vertex.

The colorability requires that the 0/1 values assigned to Boolean variables for any two adjacent vertices be distinct. Suppose that v_i and v_j are two adjacent vertices in G, we have the following constraints:

$$x_{i1} \oplus x_{j1} + x_{i2} \oplus x_{j2} = 1 \tag{2}$$

In general, there exist $|E|$ such constraints and each constraint contains p exclusive-or terms.

The feasibility problem of layer assignment is equivalent to the following Boolean satisfiability problem: find a 0/1 assignment to the $p|V|$ Boolean variables such that all the $(2^p - l)|V| + |E|$ Boolean equalities as defined in (1) and (2) are satisfied.

We note that the feasibility problem of three-layer assignment is more relevant than all the others, since it is known that four-layers are suffice for partial routings obtained from most of the current routing models, and that three-layer feasibility problem is NP-complete[12].

4 Two-Layer Routing: Signed Hypergraph Model

In this section, we show that the black-white hypergraph model can be simplified significantly under the conventional two-layer routing environment. The simplification

is carried under the assumption that a given partial routing guarantees the two-colorability of the constraint graph. This assumption is true if the original routing was done using the Manhattan model or by any other procedures that guaranteed that a two-layer realization exists.

The key concept used is a novel graph notation, called *signed hypergraph*, which is an extension of the conventional concept of hypergraph in graph theory[2]. Let $V = \{v_1, ..., v_n\}$ be a finite set of elements called *vertices*, and let $E = \{e_i | (e_i^+, e_i^-), i = 1, ..., m\}$ be a family of unordered pairs of subsets of V, where e_i^+ and e_i^- are two (possible empty) subsets of V. The couple $H = (V, E)$ is called a *signed hypergraph*, or briefly an *s-hypergraph*, if (1) $e_i \neq \emptyset$, $i = 1, ..., m$ and (2) $\bigcup_{i=1}^{m} e_i = V$. Then e_i is said to be an *edge* of H, and e_i^+ and e_i^- are called two *blocks* of the edge. All vertices in e_i are the *end-vertices* of the edge. To distinguish vertices in two blocks of e_i, we call those in e_i^+ the *positive end-vertices* and those in e_i^- the *negative end-vertices*. The number of vertices in e_i is the *degree* of e_i, denoted as $|e_i|$.

A *bipartition* π of V is a separation of V into two disjoint *groups* V_A and V_B. An edge is said to be *balanced* by a bipartition if all its positive end-vertices belong to one group, and all its negative end-vertices belong to the other group; otherwise it is said to be *unbalanced*. The *maximum balance problem* is to find the bipartition of V that maximizes the number of balanced edges.

Under the assumption that the constraint graph is two-colorable, we may condense all the vertices of a black-white hypergraph that corresponds to a connected component in the constraint graph into a single vertex, by contracting all the white edges. We may arbitrarily choose one vertex in each connected component as the representative, and all the vertices connecting to this vertex by white edges are non-representatives. A black edge may connect a set of representatives and a set of non-representatives. We distinguish these two situations by using the notation of signed hypergraph, i.e., all the representative vertices connecting to an edge are represented by its positive-end vertices, and all the non-representative vertices the negative-end vertices, or vice versa. More formally, we have the following definitions.

Definition 3 *Given a black-white hypergraph $\mathcal{H}$ of R, assume that the constraint graph G is two-colorable, then $H(R) = (V, E)$ is the signed hypergraph of R, where vertex $v_i \in V$ represents a connected component of G, and edge $e_i = (e_i^+, e_i^-) \in E$ corresponds to a black edge in $\mathcal{H}$. Moreover, if v_i connects to a black edge and v_i is a representative of a component, then $v_i \in e_i^+$; otherwise if v_i is a non-representative of a component, then $v_i \in e_i^-$.*

The constraint graph in Fig. 4 is two-colorable. There are four connected components; we represent them by 1, 2, 3 and 4, respectively. We chose vertex $a1$, $c2(b2, d2)$, $c3(b3)$ and $d3$ as representatives of each component. The resulting signed hypergraph is shown in Fig. 5.

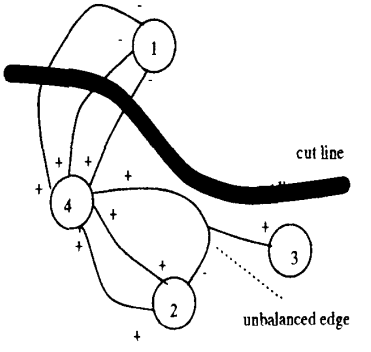

Figure 5: The signed hypergraph of routing R_1

Remark 3 *The signed hypergraph of the CVM problem is planar.*

We have the following result:

Proposition 3 *The CVM problem is equivalent to the maximum balance problem in its signed hypergraph.*

Fig. 5 illustrates one optimal solution to the maximum balance problem. Its corresponding layer assignment is illustrated in Fig 6.

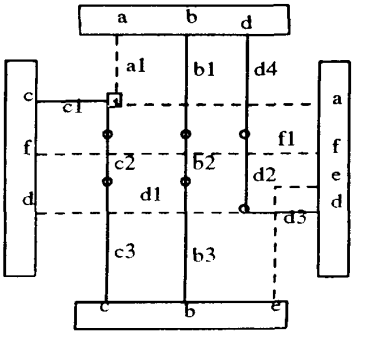

Figure 6: The complete routing solution of R_1

5 Incorporation of Various Constraints

In this section, we describe two mathematical constraints imposed on the maximum balance problem in a signed hypergraph. We show that how they can be used to model various practical constraints imposed on the CVM problem.

Fixed vertex constraints

Fixed vertex constraints specify that certain vertices must be partitioned into certain groups. They can be used to model fixed layer assignments of wire segments, for example, power lines and busses may be fixed to the metal layer in order to improve the circuit performance. In the above discussion, we assumed that all the terminals can be accessed from any layers. However, in practice, some terminals may be only allowed to be placed in certain layers. This restriction can also be modeled by fixed vertex constraints.

Path constraints

A vertex or an edge may be associated with a weight whose value depends on the partitioning of signed hypergraph. A more general form of constraints states that the partitioning must satisfy some inequalities, each of which is defined over a path in the signed hypergraph. Such constraints are called *path constraints*. A practical application of this model is performance-driven layer assignment. The current two-layer routing technology uses one metal layer and one polysilicon layer, which differ remarkably in terms of conductivity. A wire segment will have different resistance depending upon which layer it belongs to; this can be represented by weighting the corresponding vertex. A junction may have different resistance, dependent upon whether it actually corresponds to a via. Performance requirements associated with a net or associated with a path, can be modeled by path constraints, which are usually well described by a set of linear inequalities. Note that fixed vertex constraints are a special case of path constraints where a path consists of one vertex only.

The problem of bipartitioning vertices of a signed hypergraph into two groups, such that the number of unbalanced edges is minimized while satisfying a given set of path constraints, is called the *constrained maximum balance problem.*

6 Applications of the Signed Hypergraph Model

The signed hypergraph model is a robust model for the general CMV problem of two-layer routing. In this section, we mention two recent results obtained using the signed hypergraph model.

An efficient heuristic[18]

The maximum balance problem in a signed hypergraph is very similar to the maximum cut problem in a hypergraph, which is usually called the network partitioning problem. Inspired by the work of Fiduccia and Mattheyses for network partitioning, a linear-time heuristic has been developed to solve the maximum balance problem, therefore, the general CVM problem. Unlike all the previous heuristics for CVM, the proposed heuristic works directly on a signed hypergraph, instead of its estimated graph representation. Therefore, it is more efficient, and consistently obtains optimal or near-optimal results for all the tested CVM problem instances from the literature[18]. In addition, the proposed heuristic can handle fixed vertex constraints and path constraints.

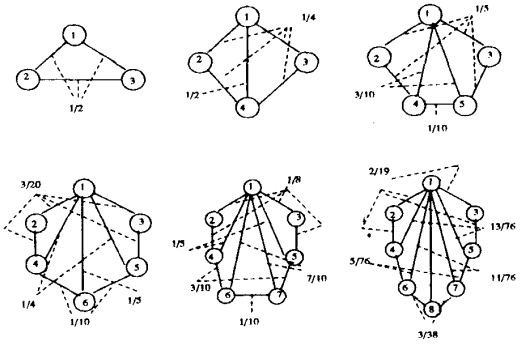

Figure 7: Fan graph modeling of k-way splits ($k \leq 8$)

Modeling of multi-way splits[19]

Using the signed hypergraph model, modeling of k-way splits is reduced to a mathematical problem of mapping the maximum balance problem in a signed hypergraph into the maximum cut problem in a real-weighted graph. Two methods are proposed for modeling a multi-way split. The *clique* method represents an edge by a complete subgraph, as used in [21, 22], but uses the weights determined by mathematical programming. The *fan* method maps an edge into a planar graph, as illustrated in Fig. 7 for $k \leq 8$. By this method, the resulting weighted graph is planar; it is the first time that applying the $O(n^{1.5}logn)$ algorithm[11] to solving the general CVM problem is possible. (The opposite is claimed in [11].) Comparisons with the methods of Stevens and vanCleemput[21], as well as Xiong and Kuh[22], are summarized in Table 1. For each k, Table 1 gives the weight, a (for the fan model see Fig. 7); the maximum error, s_∞; the probability of appearing the maximum error, p_∞; and the mean error, $\bar{s}$. By error we mean the difference of the total weights of all the edges cut by a bi-

Table 1: Comparison of Various Weighting Methods

	Stevens & vanCleemput				Xiong & Kuh				Clique method				Fan method		
k	α	s_∞	p_∞	$\bar{s}$	α	s_∞	p_∞	$\bar{s}$	α	s_∞	p_∞	$\bar{s}$	s_∞	p_∞	$\bar{s}$
3	$\frac{1}{2}$	0	1	0	$\frac{1}{3}$	$\frac{1}{3}$	1	0	$\frac{1}{2}$	0	1	0	0	1	0
4	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{3}{7}$	$\frac{1}{7}$	$\frac{1}{6}$	$\frac{1}{2}$	$\frac{4}{7}$	$\frac{3}{7}$	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{4}{7}$	$\frac{1}{7}$	$\frac{1}{2}$	$\frac{2}{7}$	$\frac{1}{7}$
5	$\frac{1}{4}$	$\frac{1}{2}$	$\frac{2}{3}$	$\frac{1}{3}$	$\frac{1}{10}$	$\frac{3}{5}$	$\frac{1}{3}$	$\frac{7}{15}$	$\frac{1}{6}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{9}$	$\frac{3}{5}$	$\frac{2}{15}$	$\frac{1}{5}$
6	$\frac{1}{5}$	$\frac{4}{5}$	$\frac{10}{31}$	$\frac{15}{31}$	$\frac{1}{15}$	$\frac{2}{3}$	$\frac{6}{31}$	$\frac{17}{31}$	$\frac{1}{9}$	$\frac{4}{9}$	$\frac{6}{31}$	$\frac{13}{93}$	$\frac{7}{10}$	$\frac{2}{31}$	0.23
7	$\frac{1}{6}$	1	$\frac{5}{9}$	$\frac{7}{9}$	$\frac{1}{21}$	$\frac{5}{7}$	$\frac{2}{21}$	$\frac{31}{63}$	$\frac{1}{12}$	$\frac{1}{2}$	$\frac{2}{21}$	$\frac{1}{9}$	$\frac{3}{4}$	$\frac{2}{63}$	0.24
8	$\frac{1}{7}$	$\frac{9}{7}$	$\frac{35}{127}$	$\frac{129}{127}$	$\frac{1}{28}$	$\frac{3}{4}$	$\frac{8}{127}$	$\frac{63}{127}$	$\frac{1}{16}$	$\frac{9}{16}$	$\frac{8}{127}$	$\frac{15}{127}$	$\frac{15}{19}$	$\frac{2}{127}$	0.24

partition and 1 (the desired value). The clique method is more accurate than the other methods. The mapping error of the fan method is no worse than the best previous clique mapping.

7 The Related Work

Various models have been proposed in the past for the CVM problem under various restrictions. The first model for the CVM problem appeared in the appendix of a 1971 paper by Hashimoto and Stevens[9]. The model is restricted to two-terminal signal nets and the grid-based two-layer channel routing environment. The early work also includes an attempt to model multi-way splits for CVM of multi-terminal-net routings by Stevens and vanCleemput [21].

For two-layer routings of two-terminal nets, Chen, Kajitani, and Chan[5], as well as Pinter[17], shown that the CVM can be characterized by the maximum cut problem in a planar graph. Using this model, a series of studies [5, 17, 11, 1] result in an $O(n^{1.5}\log n)$ algorithm for finding an optimal solution to the CVM problem, where n is the number of wire segments (more precisely the number of clusters).

During the process of deriving the above maximum cut model, various intermediate graph models have been used to capture the crossing relations and junction relations of wire segments in a partial routing, which include the layout graph of Pinter[17], the expanded graph of Barahona[1], the via-crossing graph of Chang and Du[4], and the graph model of Moliter[14]. Our black-white hypergraph is most close to Pinter's layout graph; it can be viewed as a generalization of Pinter's layout graph to routings consisting of multi-way splits. The other graph models treat potential vias as vertices.

Most of the previous models are restricted to routing of two-terminal nets. In order to describe multi-way splits resulting from routing of multi-terminal nets, Chen, Kajitani and Chan proposed a so-called topological structure. This topological structure was also used by Naclerio, Masuda and Nakajima to handle grid-less routings[15]. Due to the lack of proper representation, even the complexity study of the general CVM problem is much involved[13, 16, 6]. The idea of modeling multi-way splits by weighting two-way splits due to Stevens and vanCleemput was used by Xiong and Kuh. However, due to the lack of proper representation, both modeling methods are based on intuition and produced unnecessary approximation errors.

8 Summary

This paper attempted to give an elegant, concise, and general mathematical model of the constrained via minimization (CVM) problem arising in VLSI and PCB design. Our major purpose is to separate the mathematical aspect of the CVM from its physical details and therefore to provide an abstract model for studying the CVM problem and developing solution algorithms. The main results of this paper are:

- As far as CVM is concerned, a routing can be completely captured by a black-white hypergraph. A black-white hypergraph is a graph, but (1) each edge may connect more than two vertices; and (2) all the edges are either black or white. The CVM problem can be stated in terms of the black-white hypergraph as to find a partition of all the vertices into l-groups such that (1) all the vertices connected by a white edge belong to different groups, i.e., none of any two vertices connected by a white edge belong to one group; and (2) the number of black edges with all its vertices belonging to one group is maximized.

  A constraint graph is obtained from the black-white hypergraph by removing all the black edges. The feasibility of l-layer assignment for a given selection of potential vias is equivalent to the l-colorability of the constraint graph.

- Under the two-layer routing environment (l = 2), and under the assumption that the feasibility of layer assignment is guaranteed, the black-white hypergraph can be simplified significantly by means of the signed hypergraph. A signed hypergraph is a graph, but (1) each edge may connect more than two-vertices; and (2) all the vertices connected to an edge may belong to either of two different blocks. An edge is said to be balanced by a bipartition if all its vertices in one block belong to one group. The CVM problem of two-layer routing can be characterized by the maximum balance

problem in a signed hypergraph, i.e., finding a bipartition such that the number of balanced edges is maximized.

To illustrate the powerful of these models, we mentioned two applications of the signed hypergraph model. One is a fast and effective heuristic algorithm for the maximum balance problem. The other is modeling of multi-way splits.

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