PixelStreams-based implementation of videodetector

Marek Gorgoń, Piotr Pawlik, Mirosław Jabłoński, Jaromir Przybyło

Biocybernetic Laboratory, Department of Automatics
AGH University of Science and Technology
Al. Mickiewicza 30, 30-059 Kraków, Poland
{mago, piotrus, mjk, przybylo}@agh.edu.pl

Abstract
In the present paper the background generation and motion detection algorithms, which are of key importance for the implementation of videodetection, have been presented. A modification of the background generation algorithm, essential for proper algorithm functioning at medium and high road-traffic conditions, has been proposed. Algorithm adaptation for the implementation in reprogrammable device has been also presented. PixelStream-based implementation has been successfully performed. Real-time verification on reconfigurable platform has been done.

1. Introduction
With increasing computing power and accessibility of industrial computers and the lowering prices of monitoring devices, interest is growing in videodetection, or automated calculation of road traffic parameters, based on the analysis of videocamera image stream fed into a computer. Videodetectors, or systems located on a road crossing, consisting of several video cameras and a computer analyzing the digital images, have a considerable chance to become an alternative for induction loops commonly applied in road traffic analysis (mounted under surface of a road) [5]. With moderate additional expenses the videostreams from the cameras can be transmitted to a monitoring center, becoming a valuable source of information about possible hazards to the traffic flow. Great new possibilities are opened by the application of specialized real-time image processing devices, based on the FPGA technology. In the present stage of videodetector development it seems plausible to simulate the functioning of induction loops [1] (see Figure.1). According to the operating principle of the induction loop the vehicle detection is realized in two ways: the device detects motion and/or presence of the vehicle [6].

The detection of vehicles in motion is based on the image thresholding, realized by calculating a differential image of two consecutive frames [5]. In order to detect the immobile vehicles (e.g. waiting for the green) the differential image is analyzed, obtained by subtracting from the present frame the reference image, so called background image.

2. Modification of the background generation algorithm
Proper generation of the background image for videodetection is a necessary condition for correct realization of the vehicle detection processes. In city agglomerations, in particular for multilane arteries with high and very high traffic intensity, the correct generation of background images encounters multiple obstacles.

In work [7] the weighted average method has been applied. The background elements have been determined as local maxima of the time histograms located near the determined weighted average value.

During the analysis oriented towards transferring the described method to the intended hardware platform it has been noticed, that instead of calculation of the weighted average for each histogram, the accumulation of consecutive pixel values can be used (1). A considerable memory saving effects are obtained (the memory required is reduced 256 times!), as well as some reduction of the calculation time.
Another, much more essential modification of the weighted average method contained in work [7], was the proposition of holding the calculations of background values during the time periods, when vehicles wait for the change of traffic lights. In that period the background determination has been mutually connected with the detection of presence and motion of vehicles.

To avoid background generation for temporarily immobile vehicles, Sum of Absolute Difference (SAD) algorithm has been applied for consecutive video frames been used in order to trigger background update with particular frame. The same SAD method is used to determine the final binary signal notifying vehicle presence in one of 32 defined areas. Simplicity and robustness of SAD algorithm has been recognized in several research projects [3][4][8] especially due to its ability to be efficiently implemented in various hardware technologies for vast selections of applications fields.

The SAD algorithm for irregular regions has been implemented in the Handel-C language as a component of the PixelStream library.

3. Results of hardware implementation

Functional hardware model has been implemented in the DK4 environment and initially verified using the test vectors obtained from the model designed in Matlab/Simulink. This application used 25 PixelStreams [2] blocks in total, including user interface and host interface utilities (the presentation of the complete detailed diagram exceeds the scope of this publication). The prototype of videodetector has been realized and tested on the RC300E multimedia platform with FPGA XC2V6000 device [9].

The complete application runs in real time, i.e. it processes 25 standard PAL images with the resolution of 576 × 768 every second. The use of two output ports of the RC300E platform makes it possible to follow the generated background image and the differential image concurrently on two attached displays. Internal video streams can be also selected and displayed in run time on TFT built in panel. Computed results and statistics, (i.e. number of active pixels in specified Region Of Interest, SAD values for vehicle presence and motion, etc.) are shown on the TFT display of the RC300E platform. The results of the videodetector algorithm implementation are listed in Table 1.

4. Conclusions

In the paper, background generation algorithm has been presented for application in videodetection of vehicles. The algorithm behaviour has been examined with a test sequence including high intensity vehicle traffic. The hardware implementation of the videodetector has been done and the results are presented. The RC300 board equipped with Virtex II has been used. Software-hardware environment for real-time acquisition, processing and visualization has been successfully tested on real-time data.

The present work has been financed by the Polish State Committee for Scientific Research as a Research Project No. 4T11C01725. We wish to thank the Celoxica University Program and the Xilinx University Program for software donations.

Table 1. Results of hardware implementation.

<table>
<thead>
<tr>
<th>Resources of FPGA device</th>
<th>Used</th>
<th>% of total available</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slices</td>
<td>4,902</td>
<td>14</td>
</tr>
<tr>
<td>IOBs</td>
<td>385</td>
<td>46</td>
</tr>
<tr>
<td>Block RAMs</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>Arithmetic-Logic Gates</td>
<td>549,190</td>
<td>10</td>
</tr>
</tbody>
</table>

References