Dealing with a World of Data: A Systems Perspective

H. Peter Hofstee - IBM Austin Research Laboratory

Abstract - Increasingly Big Data computing is being applied to some of the world's most difficult, most urgent problems. This talk will describe the nature of Big Data computing and present technology that has been developed to allow Big Data computing systems to address these challenges. We discuss the design of systems for Big Data and their corresponding middleware and look at how both of these might evolve and challenge the current thinking about Big Data systems. Finally we motivate shared-memory heterogeneous architectures in this context and we discuss the coherent attach processor interface on Power 8 as a concrete example of how to achieve a system-level benefit.

Short bio - H. Peter Hofstee currently works at the IBM Austin Research Laboratory on workload-optimized and hybrid systems. Peter has degrees in theoretical physics (MS, Rijks Universiteit Groningen, Netherlands) and computer science (PhD, California Inst. of Technology). At IBM Peter has worked on microprocessors, including the first CMOS processor to demonstrate GHz operation (1997), and he was the chief architect of the synergistic processor elements in the Cell Broadband Engine, known from its use in the Sony Playstation 3 and the Roadrunner supercomputer that first broke the 1 Petaflop Linpack benchmark. His interests include VLSI, multicore and heterogeneous microprocessor architecture, security, system design and programming. Peter is an IBM master inventor with over 100 patents.
Abstract - Hobbyists have been playing with internet of things for years. They hack existing devices or 3D print their own and connect them via internet. As IoT demand is increasing, we need to find proper tools and methods to develop high quality IoT products, while maintaining the creativity of the hobbyist. The Intel Software Academic Program is working with universities to help and develop innovative student projects. We'll see what methods they use and results they achieve.

Short bio - Trained as a biologist, Paul Guermonprez worked for 8 years in the biotech field as a software developer and bioinformatician. He then joined Intel Software as an application engineer to optimize parallel software in the biotech and medical field. After 5 years, Paul took in charge the Intel Software Academic Program for the EMEA-Russia geo. The Academic program is developing technical collaborations with professors and students to make software fun and innovative. Various aspects of the program include: Hardware seeding programs, workshops, contests, mentorship. Topics covered: Internet of Things, HPC, mobile programming, perceptual computing.
Real-time Graph Exploration on Large-scale Distributed Memory Machines

Fabrizio Petrini - IBM TJ Watson Research Center

Abstract - The trend of “big data growth” presents enormous challenges, but it also presents incredible scientific and business opportunities. Together with the data explosion, we are also witnessing a dramatic increase in data processing capabilities, thanks to new powerful parallel computer architectures and more sophisticated algorithms. In this talk we describe the algorithmic design and the optimization techniques that led to the unprecedented processing rate of 15.3 trillion edges per second on 64 thousand BlueGene/Q nodes, that allowed the in-memory exploration of a petabyte-scale graph in just a few seconds. We believe that these techniques can be successfully applied to a broader class of graph algorithms.

Short bio - Fabrizio Petrini is the manager of the High Performance Analytics Department of the IBM TJ Watson Research Laboratory. His research interests include various aspects of multi-core processors and supercomputers, including high-performance interconnection networks, network interfaces, fault tolerance, and data-intensive computing algorithms for mining large data sets. He is the recipient of numerous awards for DOE, IEEE and ACM, including best paper awards from the international conference on supercomputing (SC 2003), the international supercomputing conference (ISC 2009), and the international parallel and distributed processing symposium (IPDPS 2003 and 2014).
Towards Sentient Chips: 
Self-Awareness through On-Chip Sensemaking

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Abstract:  
While the notion of self-awareness has a long history in biology, psychology, medicine, engineering and (more recently) computing, we are seeing the emerging need for self-awareness in the context of complex many-core chips that must address the (often conflicting) challenges of resiliency, energy, heat, cost, performance, security, etc. in the face of highly dynamic operational behaviors and environmental conditions. In this talk I will present the concept of CyberPhysical-Systems-on-Chip (CPSoC), a new class of sensor-actuator rich many-core computing platforms that intrinsically couples on-chip and cross-layer sensing and actuation to enable self-awareness. Unlike traditional MultiProcessor Systems-on-Chip (MPSoCs), CPSoC is distinguished by an intelligent co-design of the control, communication, and computing system that interacts with the physical environment in real-time in order to modify the system’s behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS). The CPSoC design paradigm enables self-awareness (i.e., the ability of the system to observe its own internal and external behaviors such that it is capable of making judicious decision) and (opportunistic) adaptation using the concept of cross-layer physical and virtual sensing and actuations applied across different layers of the hardware/software system stack. The closed loop control used for adaptation to dynamic variation -- commonly known as the observe-decide-act (ODA) loop -- is implemented using an adaptive, reflexive middleware layer. The learning abilities of CPSoC provide a unified interface API for sensor and actuator fusion along with the ability to improve autonomy in system management. The CPSoC paradigm is the first step towards a holistic software/hardware effort to make complex chips “sentient”.

Speaker Biography:  
Nikil Dutt is a Chancellor's Professor of CS, Cognitive Sciences, and EECS at the University of California, Irvine. He received a PhD from the University of Illinois at Urbana-Champaign (1989). His research interests are in embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, distributed embedded systems, and brain-inspired architectures and computing. He has received numerous best paper awards and is coauthor of 7 books. Professor Dutt served as EiC of ACM TODAES (2003-2008) and as AE for ACM TECS and IEEE TVLSI. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, and serves or has served on the advisory boards of ACM SIGBED, ACM SIGDA, ACM TECS and IEEE ESL. Professor Dutt is a Fellow of the IEEE, an ACM Distinguished Scientist, and recipient of the IFIP Silver Core Award.

1 Joint work with Santanu Sarma
Abstract - Smart spaces are environments such as apartments, offices, museums, hospitals, schools, malls, university campuses, and outdoor areas that are enabled for the cooperation of objects (e.g., sensors, devices, appliances) and systems that have the capability to self-organize themselves, based on given policies. Since they can be used for an efficient management of the energy consumption of buildings, there is a growing interest for them, both in academia and industry. Unfortunately, nowadays, these systems are still designed manually with ad-hoc solutions. As a consequence, a very big effort has to be spent for each new smart building. Within this context, it is interesting to investigate and realize systems able to work across different smart spaces methodologies and design tools to automate the design process of such smart spaces, in order make cheaper their realization. We are so proposing Energy Box, a compute suite for the automated design of scalable architecture for energy aware smart spaces.

Short bio - Donatella Sciuto received her Laurea in Electronic Engineering from Politecnico di Milano and her PhD in Electrical and Computer Engineering from the University of Colorado, Boulder. She is currently Vice Rector of the Politecnico di Milano and Full Professor in Computer Science and Engineering. She is in the Board of Governors of the Bank of Italy. Her main research interests cover the methodologies for the design of embedded systems and multicore systems, from the specification level down to the implementation of both the hardware and software components, including reconfigurable and adaptive systems. She has published over 200 scientific papers. She is a Fellow of IEEE and has been President of the IEEE Council of Electronic Design Automation for the past two years. She has been in the executive and program committees of different conferences and journals in the area of Electronic Design Automation.