Abstract

This paper presents the design of an integrated circuit, with a pipeline architecture, supporting programmable recursive filters intended for optimal edge detection of 8-bit images. The circuit is designed and simulated in 1.5μCmOS technology using microelectronics Computer Aided Design: COMPASS. This C.A.D. contains all necessary tools (datapath library, timing verification, chip compiler ...) for a successful design. This circuit can process up to 1024 x 1024 8-bit images at a 20MHz pixel frequency.

1 Introduction

Edge detection is an important step in image processing and analysis. It is closely related to the efficiency and robustness of a vision system. Blurred and noisy images edge detection requires recursive filters structure [1]. The design of these highly efficient filters in a single chip is very important to obtain the real time processing. The originality of the circuit lies in the following: first of all the design of an optimal edge detection for the criteria defined by Canny [2] and Deriche [3], second the pipelined architecture of the convolution unit, and finally the programmability of the circuit: the size of the image, the gradient direction and the filter coefficients. We will present in the following paragraphs the design of each block of the chip in 1.5μCmOS technology using COMPASS C.A.D. These tools use several libraries for example:

- The portable library is a set of cells that can be implemented as standard cells design.
- The datapath library is a silicon compiler that helps to create repetitive portion of our design, it is useful for implementing logic that is applied to each signal in a bus, as the convolution unit of our circuit.

2 Architecture for Second Order Recursive Filters

2.1 Presentation of the Deriche Filter

The performance of the classical edge detection algorithms based upon differential operators [3] or combining differential operators and improvement techniques [4] [5] deteriorates rapidly with blurred and noisy images. The Deriche algorithm is optimal because it gives good detection, localisation and one response to an edge. The Deriche algorithm [6] consists of calculating the first directional derivatives of the image pixels in the horizontal direction from the left to the right, then from the right to the left. The resulting image is then filtered in the vertical direction from the top to the bottom, then from the bottom to the top. The equation of the filters has two forms:

\[ X_i = a_0 I_i + a_1 I_{i-1} + b_1 X_{i-1} + b_2 X_{i-2} \] (1)

\[ X_i = a_0 I_{i-1} + a_1 I_{i-2} + b_1 X_{i-1} + b_2 X_{i-2} \] (2)

The same technique can be applied to obtain the vertical gradient. The filter size can be varied by simply changing the value of the coefficients without affecting the execution time of the algorithm. The C.P.U. time to process the 2 gradients of 256 x 256 8-bit image on Apollo DN3000 (1 MIPS) workstation is about 100s. In order to meet image analysis requirements in terms of processing speed and computing capacities, we have developed an integrated circuit with a pipelined architecture. This circuit reduces the processing time to 26ms, so we can process 37 images per second.
2.2 Functional Blocks of the Architecture

Our circuit requires the processing of only two memories: one for the initial image, and the other for the gradient image. Figure 1 shows a block diagram of the circuit which consists of 6 functional units: the coefficient register, the convolution unit, the delay line, the state machine, the counter unit and the LIFO memory.

2.3 Description of the Inputs/Outputs

The circuit functions with input 8-bits Datain, corresponding to the pixels of the memories. The Ck, RESET inputs are the clock and the reset of the circuit. Hold is an input signal to stop the sequencing of the circuit. The mode input indicates that we can load the filter coefficients or the image pixels. The Ckreg is the clock register. The newimage input allows to load a new image without changing the coefficient register. The test inputs are used to test the circuit. The input start and the output valid are used for two circuits working on parallel. The Address, AS, R/W, oeb output signals are the addresses of the memories, the address strobe, the read/write and the output enable. horiz and vertic are outputs indicating the processing step (horizontal or vertical). End is an output signal to indicate the end of the processing.

The circuit works as the following: after initialization (reset=1), we load the coefficient register (mode=0), then we load the image pixel (mode=1) so the circuit starts processing. The output end goes high when the circuit finishes processing.

3 Design of the Functional Block

3.1 The Coefficient Register

It's a serial-parallel register which is generated by using the datapath library. It includes 16 8-bit flip flops which are set up externally to supply the convolution unit with the the image size, the gradient direction and the filter coefficients.

3.2 Architecture of the Convolution Unit

The convolution unit is the most important cell in the chip, it has a pipelined architecture [7] [8] and consists of 4 identical stages placed in cascade as it's shown in figure 2.

By using the datapath silicon compiler of COMPASS, we can create repetitive portions of our design. In order to build the basic cell of the convolution unit, we...
draw a schematic by using cells from the datapath library. These cells are the multiplier, the adder and the register. A cell parameter must be created to specify the bit number in order to obtain $8 \times 8$ bit multiplier, 16-bit adder, 8-bit register and 16-bit register. See figure 4:

![Schematic of 16-bit adder cell](image)

3.3 The Delay Line
It consists of five 8-bit registers to synchronize with the convolution data.

3.4 The LIFO memory: Last In first Out
It is a 1024 16-bit static memory used to store one line of the initial image, and one line of the intermediate convolution result. Using this memory allows us to divide by two the time required to process the image. This memory is integrated in our chip by using a static RAM from the cell compiler library, with the following parameters: number of outputs, number of bits per output, seperate or common I/O, provide output enable, and several others.

3.5 The Counter Unit
It consists of several counters to address the rows and the columns of the memories.

3.6 The State Machine
It is designed to reset the circuit, generate the internal processing clock and produce the control signals of the counter unit and the external memory. This sequencer is generated by the Logic Synthesizer. We specify each state and transition in a high level language description or a state diagram. The state machine processes at $20 \text{MHz}$, has 10 inputs, 16 outputs and contains 300 equivalent gates.

4 Parallel Processors
In order to divide by two the time processing, two circuits can be cascaded to work in parallel. The communications between the two circuits are realised with the two signals start and valid as it is shown in figure 5. In fact each circuit can be programmed to work as master or slave. The start input of the master circuit is set high in order to begin reading the first line of image ($\text{RAM1}$). At the end of the line the master sets its valid output high which enables the slave circuit to start reading the second line of the initial image. At the same time the master circuit writes the convolution result of the first line in the second memory ($\text{RAM2}$). The master circuit processes the even lines and the slave circuit processes the odd lines.

![Simulation results](image)
5 The Chip Compiler

After the simulation, the circuit is placed and routed with the Chip Compiler and Layout of COMPASS. In order to generate a successful routing, we respect the following:

1. The total number of power pads placed must supply sufficient power to the I/Os and the core to cover DC and AC power dissipation in the chip. We use in our circuit 3 VDD and 4 VSS as external power pins, 4 VDD and 4 VSS as internal power pins.
2. The internal power pads are located in such a manner that we have a horizontal channel of VDD and a vertical channel of VSS. The external power pads are placed near the output pins (one pair each 10 output pins).
3. The floor plan power bus is guided manually, and its width depends on the consumption of each block.
4. In order to reduce the routing time, we use the hierarchical routing by breaking the task of routing the chip into several different routing areas, or subcells. The figure 7 shows that the subcell of the convolution unit is routed before the top.

6 Presentation of the Circuit

The circuit is designed with 33 TTL inputs and 35 CMOS outputs using 68 pin PLCC package. The figure 7 shows the packaging and the block routing of the chip. We can see in the schema from the top left to the bottom right the following blocks: the coefficient register, the lifo memory, the output adder, the standard cell block (which contains the state machine...), the convolution unit, and the counter block. The circuit area is 66.5 mm² (8.2 × 8.1) in 1.5μ CMOS technology. The approximate number of transistors is 182 thousand, the supply voltages used is 5 Volts, and the power consumption is about 750 mW.

7 Conclusion

This circuit has been designed to perform optimal edge detection by using second order recursive filters. Its pipelined structure and the possibility of parallelize allow to process at video rate. Every block of the circuit has been designed, simulated and routed with COMPASS. The circuit is fabricated in 1.5μ CMOS technology.

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References