Janusz Rajski received the Ph.D. degree in electrical engineering from Poznań University of Technology, Poland, in 1982. In June 1984, he joined McGill University, Montreal, Canada, where he became Associate Professor in 1989. In January 1995 he accepted the position of Chief Scientist at Mentor Graphics Corporation, Wilsonville, Oregon. In 2002 he became Director of DFT Engineering.

He has published more than 180 research papers in the area of silicon test and logic synthesis and is a co-inventor of 36 US and international patents. He is also the principal inventor of Embedded Deterministic Test (EDT™) technology used in the first commercial test compression product TestKompress®.

He was co-recipient of the 1993 Best Paper Award for the paper on logic synthesis published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. In 2006 he was also co-recipient of the 2006 IEEE Circuits and Systems Society Donald O. Pederson Outstanding Paper Award recognizing the paper on embedded deterministic test published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. In 2009 he received the Stephen Swerling Innovation Award from Mentor Graphics “for his breakthrough innovation, TestKompress®, and his many contributions to revitalizing Mentor's DFT business to its current position as #1 test business in EDA”.

Janusz has served on technical program committees of various conferences including the IEEE International Test Conference and the IEEE European Test Symposium. In 2007 he served as a Program Chair for ITC.

Abstract: Test compression is one of the fastest adopted DFT methodologies. It was commercially introduced eight years ago, and now it has become the mainstream DFT technology. Disruptive technology of this magnitude has impact that goes far beyond cost of manufacturing test. Test compression has changed competitive landscape, opened up completely new opportunities in product quality and yield management, and has redefined DFT technology roadmaps. It stimulates research and development activities in new areas that until now were considered not promising or not practical, enables quality of testing that was unachievable until now, accelerates adoption of new fault models that take into account physical data bases and timing information, and changes how fault diagnostics and yield learning are done in manufacturing environment.

There is a passionate debate in the professional community on the future of test compression. How scalable is it? How long will it keep up with the growing sizes of designs? What is the maximum achievable compression? How can we accommodate power constraints? What is its impact on our ability to perform diagnosis in volume production? Was it a one time deal or is it scalable solution that will be around for many generations of semiconductor technologies? Some voices focus on opportunities, others point to limitations. Some arguments are grounded in engineering others resort to financial analysis. Many of the predictions are conflicting. The presentation will discuss many of these issues, new opportunities, new and not so new challenges, as well as future technology roadmaps.