ABSTRACT

The increasing speed of digital VLSIs, like microprocessors, has dictated the use of more than one connection to the ground and supply voltage per package. Multiple power connections will guarantee the required noise immunity. However, proving that all these pins are correctly connected on a board is almost impossible. In this paper a solution to this problem, which uses the boundary scan method, is presented.

INTRODUCTION

Due to the competitive market, system companies are forced to enhance the performance of their products continuously. More functionality at a higher speed should fit into a smaller volume with less power consumption.

To fulfill these conflicting demands the electronics industry has sought solutions in the direction of process technology and packaging. Examples of these are: increasing complexity of Integrated Circuits and higher package densities by means of Surface Mount Devices. In [1] it is shown that these technologies are approaching their physical limits.

An other way to improve the performance of a system is by increasing the clock rate. However, due to parasitic effects there is an upper limit to the clock rate. This upper limit can be pinpointed at component level, a certain component is the weakest link in a chain.

TESTABILITY PROBLEM

To increase the clock rate of a component the parasitic effects must be countered by adding multiple power pins to a package. Because these multiple power connections are electrically parallel, a new problem arises during Printed Circuit Board (PCB) assembly. Not connected power pins cannot be detected by the current PCB test methods. However to assure reliable system operation these connections must be tested for 100% in the production flow as soon as possible.

The testing issues during the several stages the component's life will be considered: IC-design, IC-production, PCB-design, PCB-assembly and system-use.

3.1 IC-design

During this phase the maximum clock rate, the number of simultaneously changing outputs and maximum currents together with the process technology are considered. Taking all these variables into account a minimum number of pins per power supply connection are assigned. A conflict might arise if sufficient pins are not available on a certain package type. Then a trade-off must be made: less pins or a more expensive package. Multiple power pins are described in the data sheets. Testability of the power connections is up till now not considered by the designers.

3.2 IC-production

At this stage each IC package pin is separately accessible. Testing these multiple power pins after bonding and assembling the die into a package is a matter of ohmic measurement. Diagnostics is good, and bad products are discarded.

3.3 PCB-design

In this phase the PCB-designer has to read the data sheets carefully and if he is lucky an advise on how to design this component onto a PCB is given. Sometimes even a PCB lay-out is supplied, depicting the exact shape of the power supply connections on a PCB. Testability of the power connections is not considered.
3.4 PCB-assembly

Digital VLSIs are supplied in a great variety of packages, ranging from Dual In Line (DIL), Leadless Chip Carrier (LCC) to Pin Grid Array (PGA). After placing and soldering a component onto a PCB the PCB must be tested.

From [2] it is known that 'opers' and 'shorts' are responsible for the majority of the faults on a board, and that these faults can be detected almost completely (99.8%) by ir-circuit testing. For components with a single power connection the correctness of this connection is inherent to the good functioning of this part.

Testing in an electrical way is still the only reasonable alternative, because for instance visual testing of a PGA is still impossible. Probing can only be done on the PCB-side of the power connection and not inside the component! Testing the multiple power connections between a component and a PCB, using in-circuit testing, is therefore impossible.

Functional testing seems to offer some possibilities. An error in the power connections will only show up during extreme clock rate, power and temperature conditions. So, it must be possible to influence these conditions. This has some serious price consequences for the functional tester. If an error is encountered by the functional tester, the exact location of the fault cannot be extracted from the error message. Diagnostics is poor or even impossible.

Concluding, the limitations of functional testing are a long preparation time and weak diagnostics, in-circuit testing is limited by the need to have access to the device under test. Therefore, both test methods do not offer practical solutions so the class of faults under discussion must be classified as untestable.

3.5 System-use

Errors encountered during system operation are extremely difficult to locate. So tracing and repair is very expensive.

4 CONFIGURATION OF POWER PINS

Several ways of applying power to a core of an VLSI can be recognised. The simplest configuration is one Ground and one Power pin.

A schematic of a component on a board with the simplest power configuration is drawn in figure 1a.

The model of figure 1a also applies if a core is subdivided into more parts and each part has its own power connections.

A component with two Ground pins and two Power pins is drawn in figure 1b. For more complex designs and bigger packages this number may increase considerably. For example the Intel 80386 has 20 Vcc and 21 Vss pins in the Pin Grid Array package.

4.1 Electrical Representation.

The physical power supply connections can be distinguished into three parts: a copper part on the PCB, an interconnection part and a aluminum part within the IC package, see fig 2.

The power connections are schematically drawn in figure 3.

fig. 2

fig. 3

Cu = Copper  Al = Aluminum
T = solder + lead + bonding wire
Because there are no principal differences between the physical Vdd and Vss connection, only one circuit will be described. The resistance properties of the Copper (Rcu) and Aluminum (Ral) tracks are important for further discussion.

From a typical connection on a PCB it was found that the value of Rcu lies in the range of 5 to 25 milli-ohms. In the case of a full copper layer values of less than 1 milli-ohm may be expected.

The value of Ral depends on the lay-out of the power tracks on the die. A typical estimation of the resistance of an aluminum track can be made as follows: suppose

- track length L
- track width W
- \( R_{sq} A1 = 60 \text{ mohm/sq} \) \( (sq = \text{square}) \)

\[ R_{al} = R_{sq} A1 \times \frac{W}{L} = 0.6 \text{ to } 3 \text{ ohms}. \]

Comparing the value of Rcu to the value of Ral a two decade difference can be observed. The resistance of the solder pad, IC lead and bonding wire is for clarity included into Rcu. This resistance difference can be used to discern a good connection from a bad one.

4.2 Practical Verification

The above suppositions were verified on a 68000 processor by measuring the ohmic resistances between the power pins of each supply connection. Three different packages from several manufacturers were available: DIL, PLCC and PGA. Table 1. lists the power supply pin numbers for the three package types of the 68000.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>GND pins</th>
<th>Vcc pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIL</td>
<td>16, 53, 56, 57</td>
<td>14, 52, D2, E9</td>
</tr>
</tbody>
</table>

Table 1.

Table 2 lists the resistances measured between the package pins of each power connection per package type.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>GND pin</th>
<th>R (ohms)</th>
<th>Vcc pin</th>
<th>R (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIL</td>
<td>16, 53</td>
<td>1.2</td>
<td>49</td>
<td>3.4</td>
</tr>
<tr>
<td>PLCC</td>
<td>16, 17</td>
<td>i</td>
<td>14, 52</td>
<td>3.4</td>
</tr>
<tr>
<td></td>
<td>16, 56</td>
<td>i</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16, 57</td>
<td>i</td>
<td>13.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>17, 57</td>
<td>i</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PGA</td>
<td>82, D9</td>
<td>1.1</td>
<td>D2, E9</td>
<td>1.6</td>
</tr>
</tbody>
</table>

(i-infinite)

Table 2.

The values measured conform very well to the previous estimates, except in the case of the PLCC package, 13.6 ohms! This rather high value was measured on all samples of all manufacturers.

4.3 A Real-life Case

The reasons to use multiple power connections were given earlier. Regarding the resistance values of table 2 and the power dissipation of the 68000 [3] of 0.4 Watts a voltage should be present across the pins if one of them is interrupted. To verify this, a small 68000 system was used to do some measurements. This system, an Educational Computer Board [4], contained a 68000 4MHz in DIL package.

By disconnecting one of the GND pins of the 68000 from the Ground of the system the noise voltage induced by the current spikes could be observed. An average voltage of 120 mV and a peak voltage of 1.5 V was measured between the two GND pins of the IC! For a 12 MHz version the values were: average 170 mV, peak 1.8 Volt. These measurements, when done under normal ambient and power supply conditions, did not disturb the system behaviour. However, varying the temperature or power supply within the allowed range did disrupt the processor.

The conclusion, from the above experiments, is that bad power connections are indeed dangerous for system performance during extreme conditions. Parts of the logic have to operate with a reduced power supply voltage and an increased noise sensitivity.

5 TESTING STRATEGY

From the estimation and the practical measurements made, the conclusion is that in the case of a 'open' in a multiple connection power supply, a voltage difference will exist between the pins of such a multiple power supply connection. This voltage, in the range of 100 mV can be used to diagnose the fault on a board.

Using a scratch-probe on a tester is one possibility. However, the shape of the package (PGA) and the location of the fault (bonding wire) will make this method useless in most cases.

To test and diagnose a fault three basic steps must be taken: measure a voltage, convert it to a digital value and observe this digital value.

By using the resistance difference noted in figure 3 and by adding some extra logic into the component a method has been developed to detect this class of faults. Two ways of measuring and converting the error voltage into a digital value will be presented.

The observability of the internal digital signals can be solved by the boundary scan method.
5.1 Boundary Scan

The boundary scan method is a technique specially aimed at board testing to find process errors made during the production phase of a board [5],[6]. In essence boundary scan may be regarded as an 'electronic pin bed' with three modes of test operation: external, internal and sample test mode. The external test mode is aimed at testing the board interconnect, the internal test mode at the core of the IC. With the sample mode operations like a logic analyzer measurement are possible during system operation.

This structured technique can find and pinpoint among others all the soldering faults in the functional connections of a board. Power supply pins will, as the other pins, have their equal contribution of faults. Up till now, no provisions have been made in the boundary scan methodology to test this class of faults.

5.2 RAM Sense Amplifier

The voltage present across the aluminum track inside the IC must be converted to a digital value. A low voltage (< 10 mV) is an indication of a good connection. A higher voltage (>100 mV) indicates a faulty one.

One way to convert this voltage to a digital value is by using an element like a RAM sense amplifier. RAM sense amplifiers can sense and convert a small analogue voltage to a digital value. The sensitivity of these types of amplifiers lies in the wanted range. The digital value can directly be fed into the input of a boundary scan flip-flop. By means of the boundary scan path the result can be shifted out to the external test equipment, as shown in figure 4.

Extra attention must be paid to the power supply of the sense amplifier. To guarantee a correct power supply level, in the case of a fault, a separate track in parallel to the system track will be needed.

5.3 Flip-flop Sensor

Another way to convert an analogue value into a digital value is by using a flip-flop as a sensor. This technique, as explained in [7], employs a flip-flop brought to its unstable state. An imbalance, introduced by the voltage to be measured, will change the probability of a 'one' or a 'zero' output. Integrating over many cycles will deliver a definite answer on the occurrence of a fault.

Integrating can be done on the tester, however many shift operations may be required through the boundary scan path. Therefore integrating must be done locally. Extra hardware will be needed.

6 CONCLUSIONS

A class of faults, which so far was not testable, was proven to exist both in theory and in practice. These faults, introduced by the use of multiple power connections on one IC, should be eliminated during the production of high quality systems.

Two solutions were presented, which require the addition of some extra detection and conversion logic per power pin. Both solutions fit into the boundary scan method.

Further research will be needed to make available the proposed solutions for the wide variety of technologies.